42V, 3A Synchronous Step-Down Regulator with 5μA Quiescent Current

AWK6809

FEATURES

- Wide Input Voltage Range: 3.0V to 42V
- Adjustable and Synchronizable: 200kHz to 2.2MHz
- 3A Output Current Capability
- Ultralow Quiescent Current Burst Mode Operation:
  <5μA (Typ.) from $12V_{IN}$ to $3.3V_{OUT}$
- Output Ripple <$10mV_{P-P}$
- Peak Eff. **>92.5%** at 1A from $12V_{IN}$ to $5V_{OUT}$
- Minimum On Time: **35ns** (Typ.)
- Low Dropout
- Peak Current Mode Operation
- Spread Spectrum Frequency Modulation for low EMI Operation
- Programmable Soft Start and Tracking
- Internal Compensation
- Frequency folded back when short circuit

APPLICATION

- Consumer systems: Robotic Vacuum Cleaner, Drone.
- Battery Powered System: Power Tools, Home Appliance, Drone, GPS Tracker etc.
- Industrial and Medical Power Supplies

DESCRIPTION

The AWK6809 is a high efficiency synchronous monolithic step-down switching regulator with integrated internal high-side and low-side MOSFETs. It provides up to 3A output current with peak current mode control for fast loop response.

The AWK6809 operates over a wide input voltage range from 3.0V to 42V with only 5uA ultralow quiescent current. It is ideal for automotive input environments and battery power system due to its extremely low quiescent current.

Spread spectrum frequency modulation is adopted in AWK6809 for low EMI operation, standard features include soft start (SS), external clock synchronization (SYNC), enable (EN) control and power good (PG) indicator.

During output short circuit, the switching frequency is folded back when the output is lower. In addition, the current through the low-side MOSFET is monitored to prevent the inductor current from running away. Thermal shutdown provides reliable and fault-tolerant operation.

Device Information

DEVICE	PACKAGE	BODY SIZE(NOM)
AWK6809	DFN-10L	3.00mm × 3.00mm
AWK6809	EMSOP-10L	3.00mm × 3.00mm

TYPICAL APPLICATION

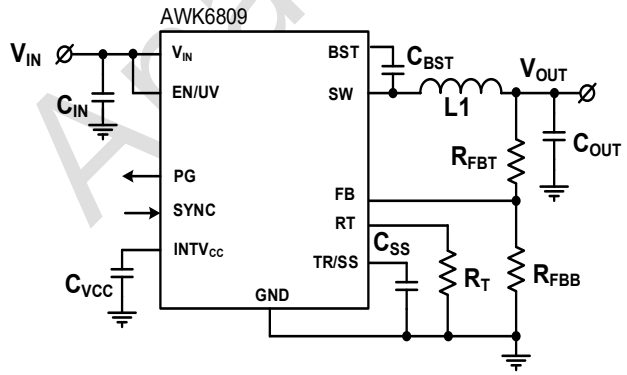

Fig.1 Schematic Diagram

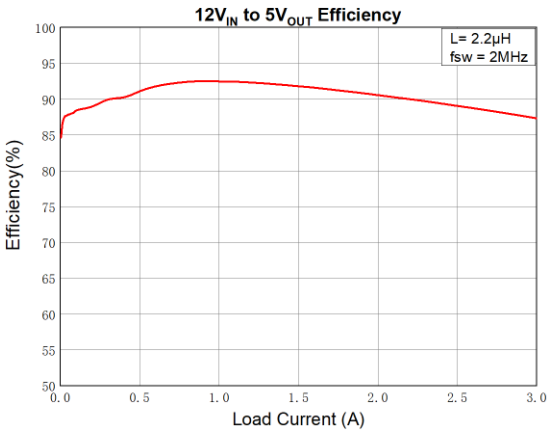

Fig.2 Efficiency vs. Output Current

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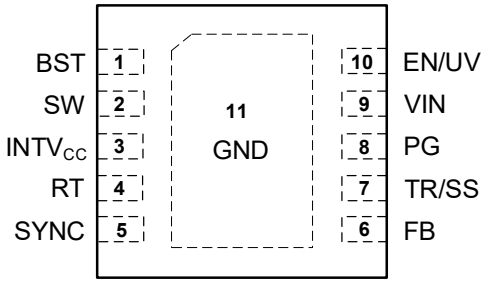
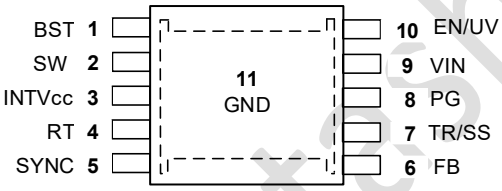
PIN CONFIGURATION

Package	Pin Configuration (TOP VIEW)
DFN-10L	
EMSOP-10L	

PIN DESCRIPTION

Table 1. Package Pins Description(1)

No.	Pin	Type(2)	Description
1	BST	I/O	Boot-strap supply voltage for internal high side driver
2	SW	I/O	Switching Node Output
3	$INTV_{CC}$	O	Internal 3.5V power supply for internal control circuits. A 1uF decoupled ceramic capacitor is recommended to connect this pin.
4	RT	I	A Resistor to Set the Switching Frequency. Refer Table 2 for the details.
5	SYNC	I	External Clock Synchronization Input. Ground this pin for Burst Mode at light load. Leave floating for Pulse-skipping Mode without spread spectrum modulation. Tie to $INTV_{CC}$ or a voltage between 3.2V to 5.0V for Pulse-skipping Mode with spread spectrum modulation.
6	FB	I	Feedback Sensing Input
7	TR/SS	I/O	Output Tracking and Soft Start. A TR/SS voltage below 0.782V forces the regulator to regulate the FB voltage to equal the TR/SS voltage.
8	PG	I/O	Power Good. Open drain power-Good flag output. High= power OK, Low= power bad.
9	VIN	P	Input Supply to Regulator. Connect a bypass capacitor to this pin.
10	EN/UV	I	Enable Input or Shutdown Input. An external resistor divider from V_{IN} is used to program a V_{IN} enable and shutdown threshold.
11	GND	G	Exposed Ground Pad

(1)The pin order and functions of DFN - 10L and EMSOP - 10L are the same.

(2) G = Ground, I = Input, O = Output, P = Power

ABSOLUTE MAXIMUM RATINGS

		Min	Max	Units
Input Voltages	VIN, EN/UV, PG to GND	-0.3	42	V
	FB, TR/SS, SYNC, RT to GND	-0.3	5.5	
	BST to SW	-0.3	5.5	
Output Voltages	SW to GND	-0.3	42	V
	VCC to GND	-0.3	5.5	
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	

RECOMMENDED OPERATING CONDITIONS

		Min	Max	Units
Buck Regulator	VIN	3.0	42	V
	SW		42	
	FB, SYNC, TR/SS	0	5	
Control	EN	0	42	V
	PG	0	42	
T_J	Junction temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM	±2000	V
	CDM	±500	

ELECTRICAL CHARACTERISTICS

Limits apply over the recommended operating junction temperature range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12 V. V_{OUT} is converter output voltage.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply						
V_{IN_MIN}	Minimum Input Voltage			2.8	3.2	V
I_{SHDN}	Shutdown Supply Current	V_{EN}=0V, V_{SYNC}=0V		1	4	μA
I_Q	Operating Quiescent Current	V_{FB} =0.82V V_{EN}=2V		1.5	7	μA
I_{SUPPLY}	Input Supply Current In Regulation	V_{IN}= 6V, V_{OUT} = 2.7V, I_{OUT} = 100uA		54		μA
MOSFETs						
R_{DSON_H}	High Side MOSFET ON Resistance			175		mΩ
R_{DSON_L}	Low Side MOSFET ON Resistance			110		mΩ
I_{LIMIT_H}	High Side MOSFET Current Limit (1)		4.2	5.5	6.7	A
I_{LIMIT_L}	Low Side MOSFET Current Limit (1)(2)		3			A
I_{SW_LKG}	SW Leakage Current	V_{IN} = 42V, V_{SW} = 42V			10	μA
Enable						
V_{EN_H}	Enable High Threshold			1.08	1.11	V
V_{EN_L}	Enable Low Threshold		0.82	0.845		V
V_{EN_HYS}	Enable Hysteresis Threshold			225		mV
I_{EN}	EN Pin Leakage Current	V_{EN} = 2V			50	nA
SYNC						
V_{SYNC_L}	Sync Low Input Voltage		0.5	0.8		V
V_{SYNC_H}	Sync High Input Voltage			2.85	3.2	V
f_{SSM}	Spread Spectrum Modulation Frequency		1	3	6	kHz
SOFT START						
I_{SS}	TR/SS Source Current		1	2	3	μA
R_{SS_DW}	TR/SS Pull-Down Resistance			230	500	Ω

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Feedback						
V_{REF}	Feedback Reference Voltage		0.770	0.782	0.794	V
I_{FB}	Feedback Pin Input Current	V_{FB} = 0.782V			50	nA
Power Good						
V_{PG_HR}	PG High Threshold Rising	% of V_{FB}	106	111	115	%
V_{PG_HF}	PG High Threshold Falling	% of V_{FB}	104	109	113	%
PG_{HYS_H}	PG Hysteresis High	% of V_{FB}		2		%
V_{PG_LR}	PG Low Threshold Rising	% of V_{FB}	89	92	95	%
V_{PG_LF}	PG Low Threshold Falling	% of V_{FB}	87	90	93	%
PG_{HYS_L}	PG Hysteresis Low	% of V_{FB}		2		%
I_{PG}	PG Pin Leakage Current	V_{PG} = 42V			700	nA
R_{PG}	PG Pull-Down Resistance	V_{PG} = 0.1V		450	1000	Ω
V_{IN-PG}	Min. Input Voltage for PG Function				1.8	V
Switching Frequency Timing						
f_{SW}	Switching Frequency	R_T=221k	155	200	245	kHz
		R_T=60.4k	640	700	760	kHz
		R_T=18.2k	1875	2000	2125	kHz
T_{ON_MIN}	Min. Turn On Time (1)			35		ns
T_{OFF_MIN}	Min. Turn Off Time			95		ns
Thermal						
T_{SD}	Thermal Shutdown			165		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			15		°C

(1) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

(2) Derived from bench characterization. Not tested in production.

TYPICAL CHARACTERISTICS

Unless otherwise specified the following conditions apply: V_{IN} = 12V, f_{SW} = 2MHz, L=2.2μH, C_{OUT} =44μF, T_J =25°C

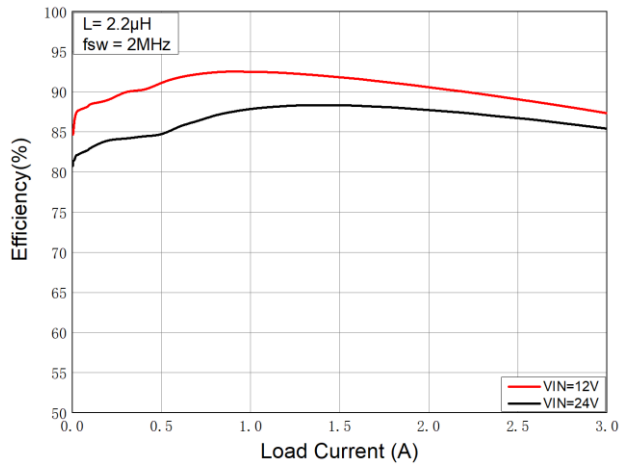


Fig.3 Eff. VS Load Current when V_{OUT} = 5V, Burst Mode Operation

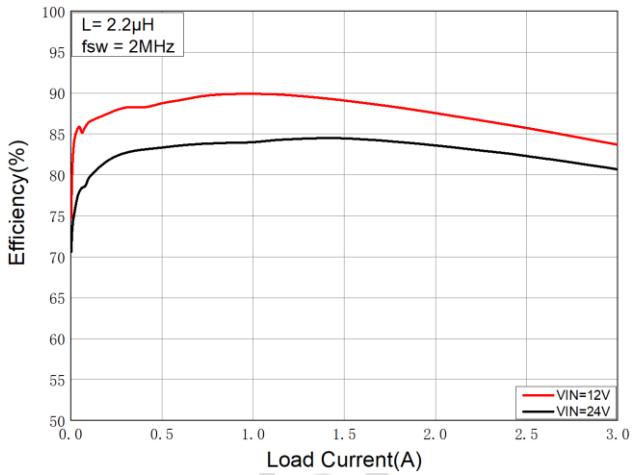


Fig.4 Eff. VS Load Current when V_{OUT} = 3.3V, Burst Mode Operation

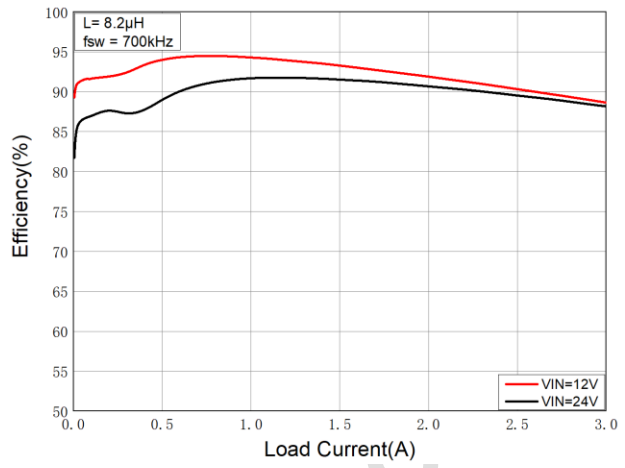


Fig.5 Eff. VS Load Current when V_{OUT} = 5V, Burst Mode Operation

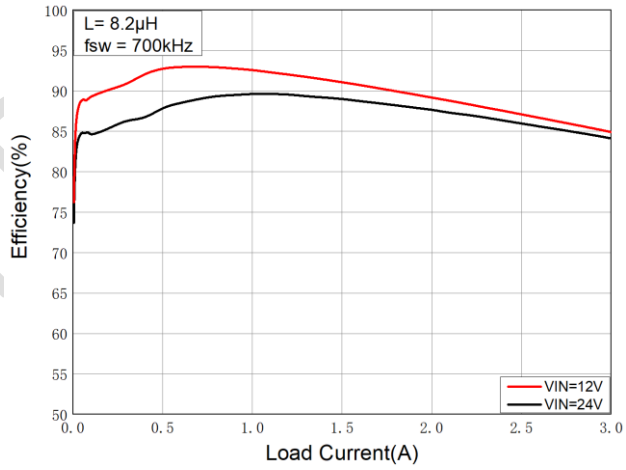


Fig.6 Eff. VS Load Current when V_{OUT} = 3.3V, Burst Mode Operation

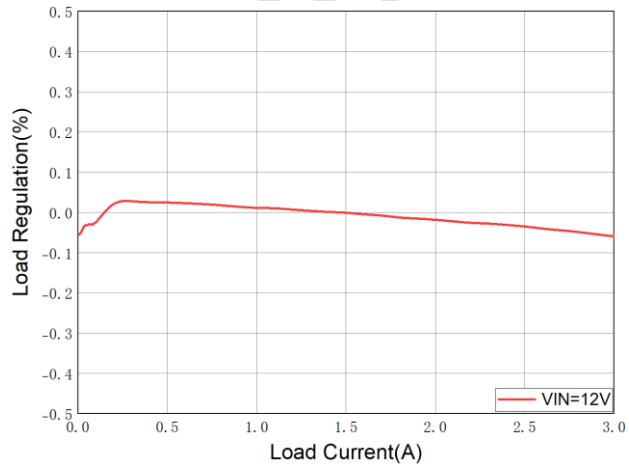


Fig.7 Load Regulation when V_{OUT} = 5V

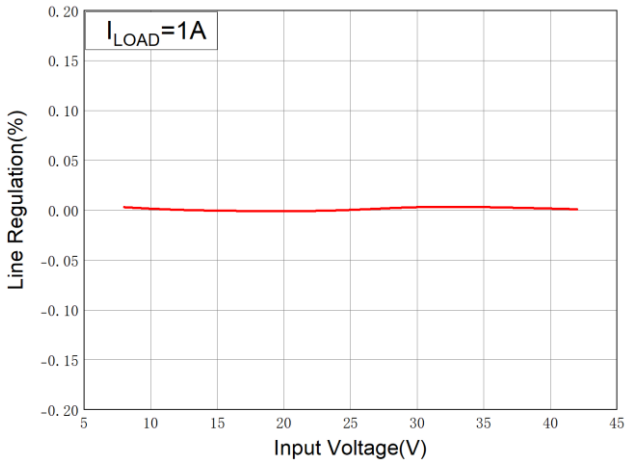


Fig.8 Line Regulation when V_{OUT} = 5V

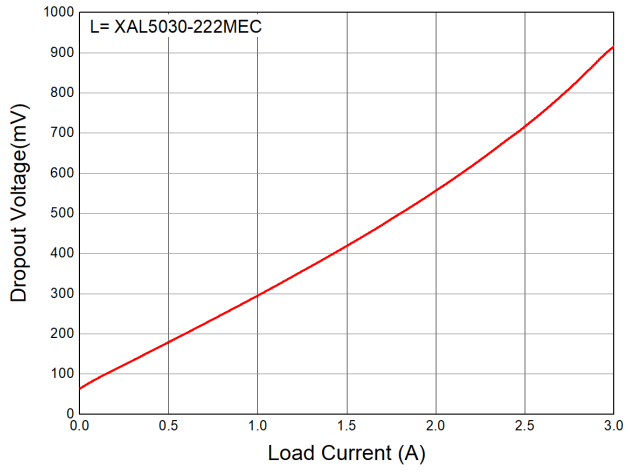


Fig.9 Dropout Voltage with Load Current

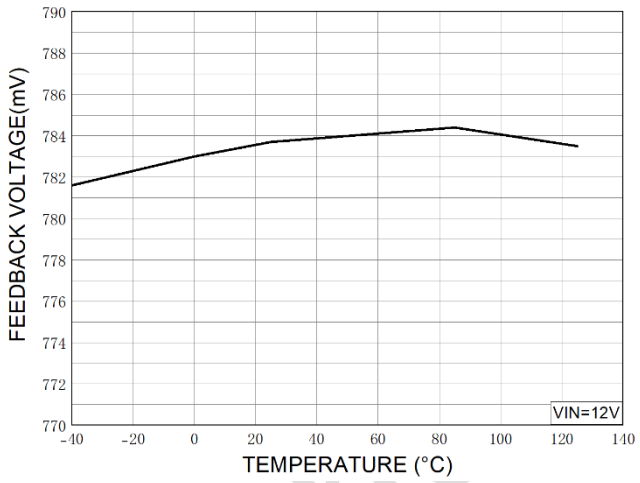


Fig.10 Feedback Voltage with Temperature when V_{IN} = 12V

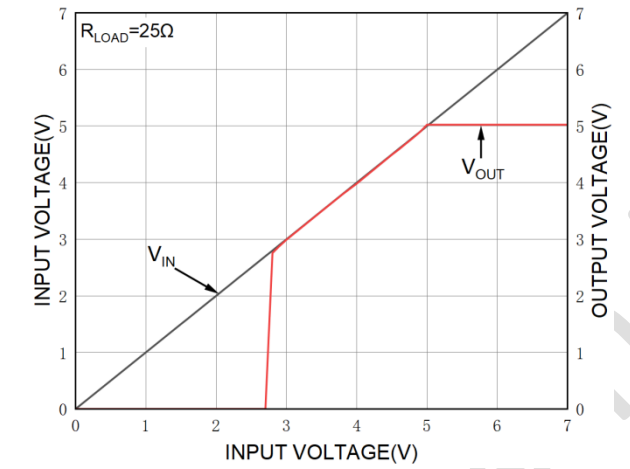


Fig.11 Start-Up Dropout

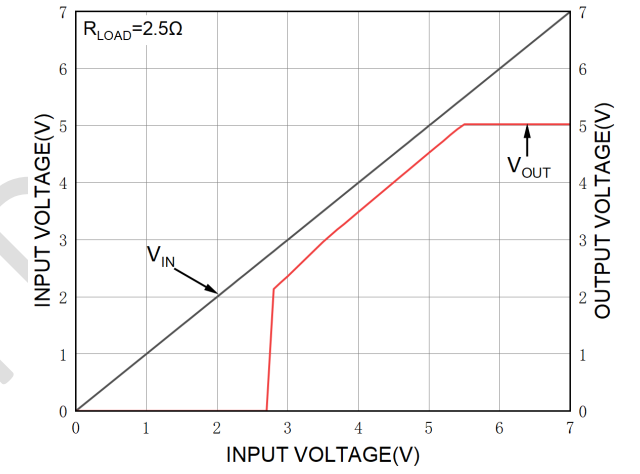


Fig.12 Start-Up Dropout

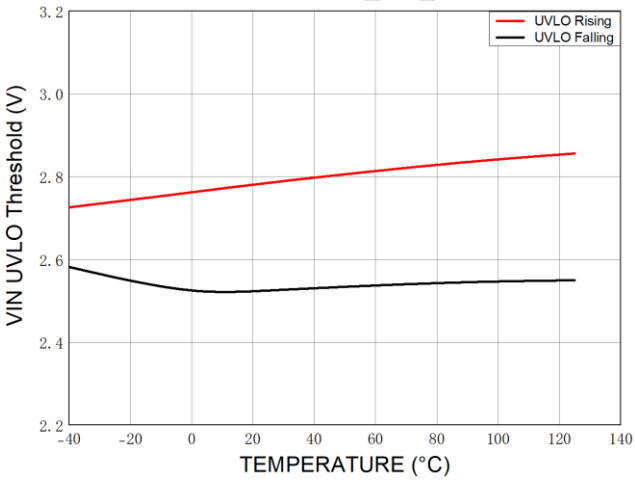


Fig.13 VIN UVLO with Temperature

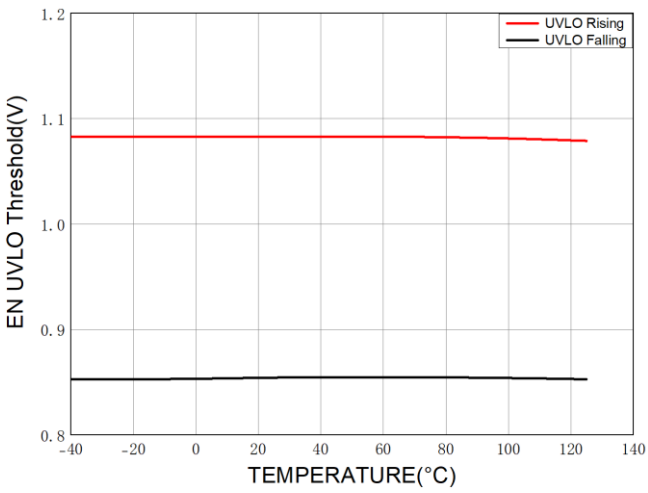


Fig.14 EN UVLO with Temperature

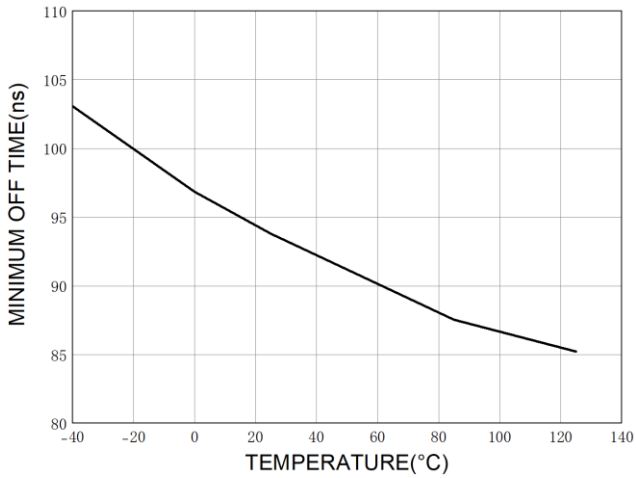


Fig.15 Minimum Off Time with Temperature

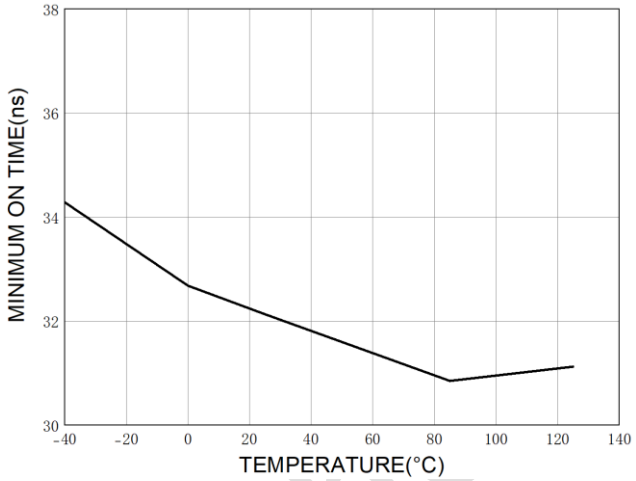


Fig.16 Minimum On Time with Temperature

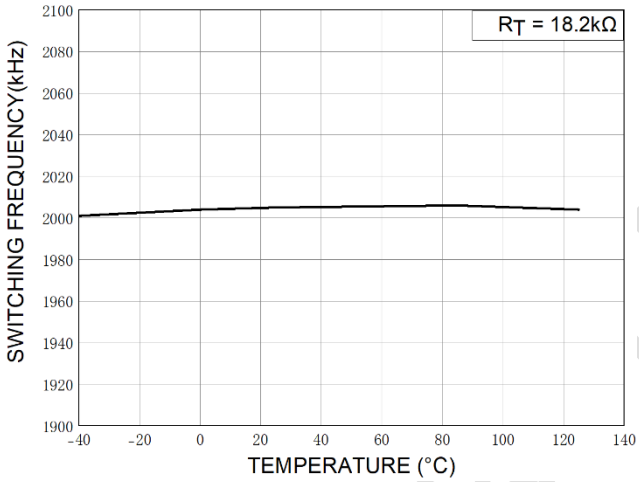


Fig.17 Switching Frequency with Temperature

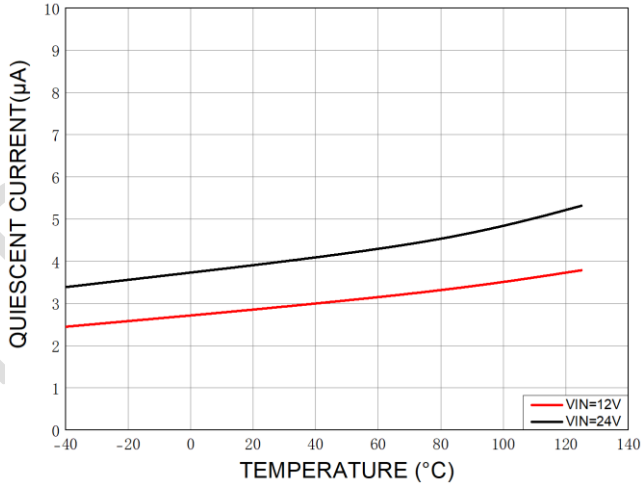


Fig.18 No-Load Quiescent Current when V_{OUT}=3.3V

BLOCK DIAGRAM

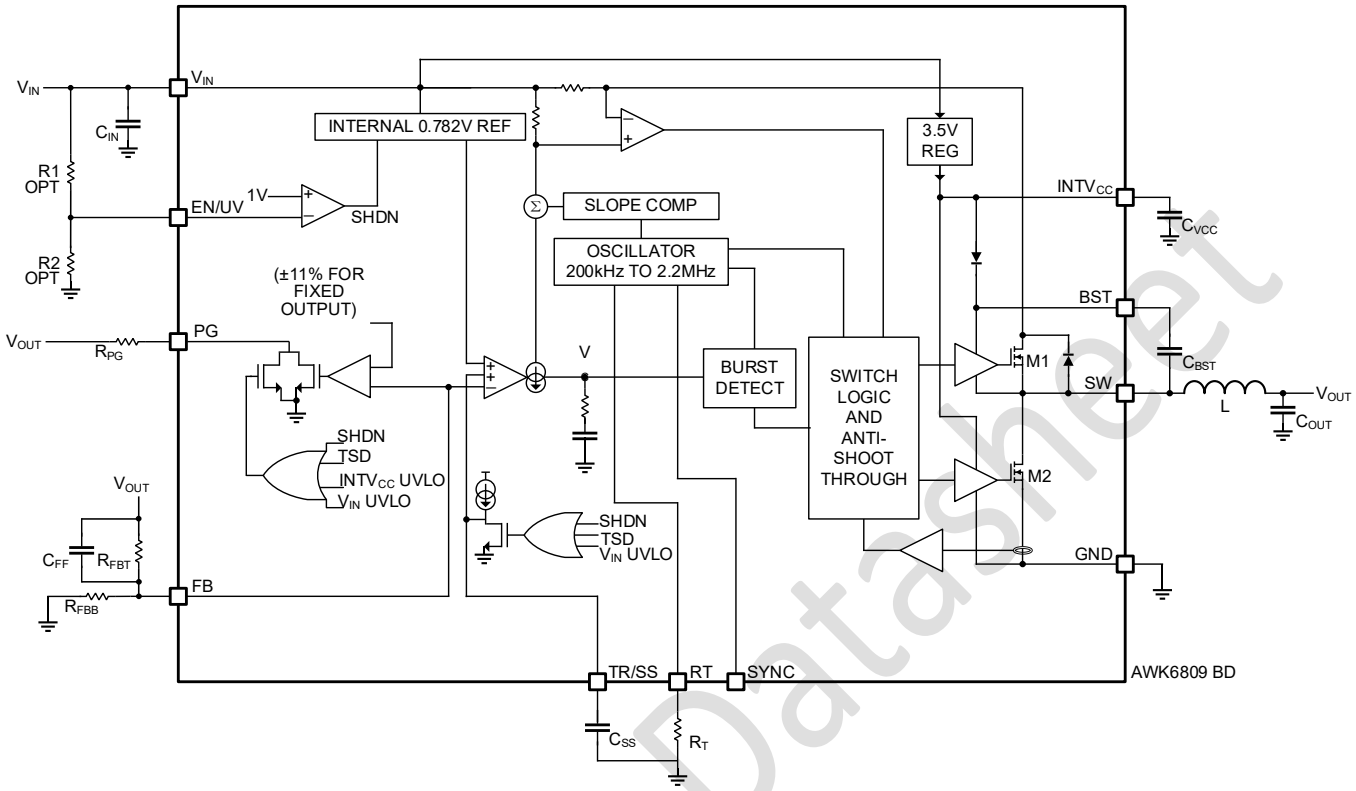


Fig.19 AWK6809 Block Diagram

PRODUCT OVERVIEW

The AWK6809 is a synchronous, step-down, switching regulator with integrated high-side and low-side power MOSFETs. The AWK6809 can provide 3A of output current with very high efficiency from light load to full load. The AWK6809 features a wide input voltage from 3.0V to 42V, the switching frequency are from 200kHz to 2.2MHz. The programmable soft start limits inrush current during power starts. The AWK6809 also integrated compensation circuit inside the chip to simplify the loop design. Another highlighted feature is its very low operational quiescent current which makes it suitable for battery powered applications.

SYNC Pin Function

The SYNC pin provides multiple control modes for switching frequency operation. When grounded (below 0.4V), the device enters a burst mode operation, reducing the switching frequency under light-load conditions to improve efficiency. Leaving the pin floating configures the device for pulse skip mode, ensuring switching occurs every cycle even under light load. Applying a high-level voltage (between 3.2V and 5V) enables pulse skip mode with an additional frequency jitter function, introducing approximately 3kHz of modulation to mitigate EMI. Furthermore, the AWK6809 switching frequency can be synchronized by an external clock (with a duty cycle of 20% to 80%, a low level below 0.9V, and a high level between 2.7V and 5V) to the SYNC pin. It should be noted that the external clock frequency must be higher than the oscillator frequency programmed by the RT pin.

Enable Pin

The AWK6809 is disabled when EN pin is low and is enabled when EN pin is high, the rising threshold of EN is 1.08V, with 225mV hysteresis window. The EN pin can be tie to VIN pin when shutdown function is not required, or tie to a logic level if shutdown control is required. Do not leave EN pin floating.

Adding a resistor divider from VIN to EN programs the AWK6809 to keep output voltage in regulation when input voltage is above desired voltage. Besides, this threshold voltage is used shutdown the device when VIN is shorted or current limited to prevent further damage to the device. The $V_{IN(EN)}$ threshold is adjusted by setting the value of R1 and R2 in Fig.19 using the following equation:

$$V_{IN(EN)} = \left(\frac{R_1}{R_2} + 1\right) \times 1.08$$

where the AWK6809 is remained off as long as VIN is lower than $V_{IN(EN)}$. Due to EN comparator hysteresis, the device will be active when VIN is slightly higher than $V_{IN(EN)}$.

Attention should be paid when the device is operating in light-load Burst Mode, the current flows through VIN(EN) resistor to ground cannot be neglected if high efficiency is required, therefore, the VIN(EN) resistors should be large to minimize their effect on light-load efficiency.

Power Good Indication

The AWK6809 features an open-drain power-good output (PG) to monitor the output voltage status. It can be pulled up to either $INTV_{CC}$ or V_{OUT}, through a 100kΩ resistor, as desired. If The power-good function is activated after soft start is finished and is controlled by a comparator connected to the feedback signal V_{FB}.

If V_{FB} rises above a power-good low threshold (V_{PG_LR}) (typically 92% of the reference voltage), the voltage on PG pin will be held high. When V_{FB} exceeds V_{PG_HR} (typically 111% of the reference voltage), the PG pin will be pulled low. If V_{FB} falls below a power-good high threshold (V_{PG_HF}) (typically 109% of the reference voltage), the voltage on PG pin will be held high. When V_{FB} exceeds V_{PG_LF} (typically 90% of the reference voltage), the PG pin will be pulled low. The power good indication is shown in Fig.20.

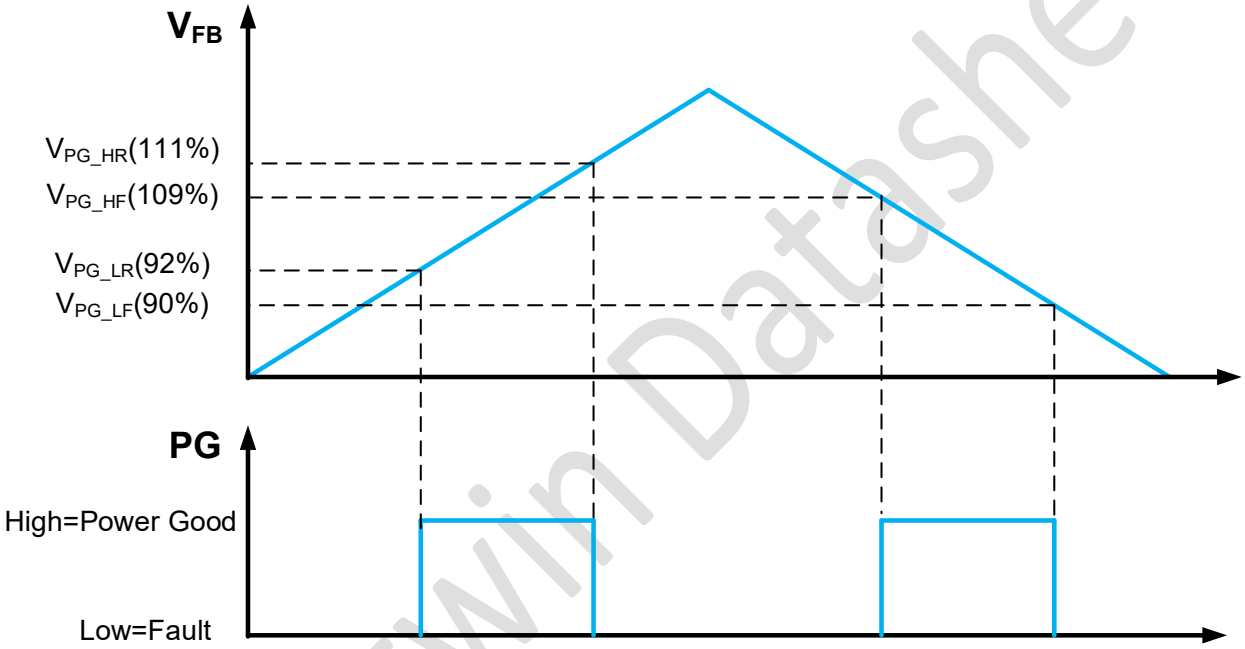


Fig.20 Power Good Operation

$INTV_{CC}$ Regulation

An internal low dropout (LDO) regulator generates the 3.5V supply voltage from input voltage to deliver power for drivers and internal bias circuitry, a ceramic capacitor with at least 1uF capacitance should be placed close to INTVcc pin to provide good bypassing to ground. Do not connect any external load to INTVcc pin.

Output Voltage Tracking and Soft-Start

The AWK6809 allows user to program its output voltage ramp rate by means of TR/SS pin. An internal 2uA current source pulls up the TR/SS pin to $INTV_{CC}$. Putting an external capacitor on TR/SS pin enables the soft-start function to prevent large input surging current. During startup, the output voltage proportionally tracks the TR/SS pin voltage, from 0V to 0.782V, instead of the internal 0.782V voltage reference, the TR/SS pin voltage serves as the reference to the error amplifier, regulating the output voltage, when TR/SS pin voltage is above 0.782V, tracking is disabled and internal 0.782V voltage reference serves to regulate the output voltage.

Short Circuit Protection

The AWK6809 will tolerate a shorted output. There are two features used for protection during output short-circuit. First, the switching frequency will fold back when the output voltage is below the set point to maintain inductor current control. Second, the system continuously monitors the low side MOSFET current. If the inductor current exceeds safe levels, the turn-on of high side MOSFET will be delayed until the inductor current returns to a safe range.

APPLICATION INFORMATION

Fig.21 shows a typical application circuit for the AWK6809. Thanks to the high integration in the AWK6809, the application circuit based on AWK6809 only need input capacitor, output capacitor, output inductor and feedback resistors which are needed to be selected based on applications specifications.

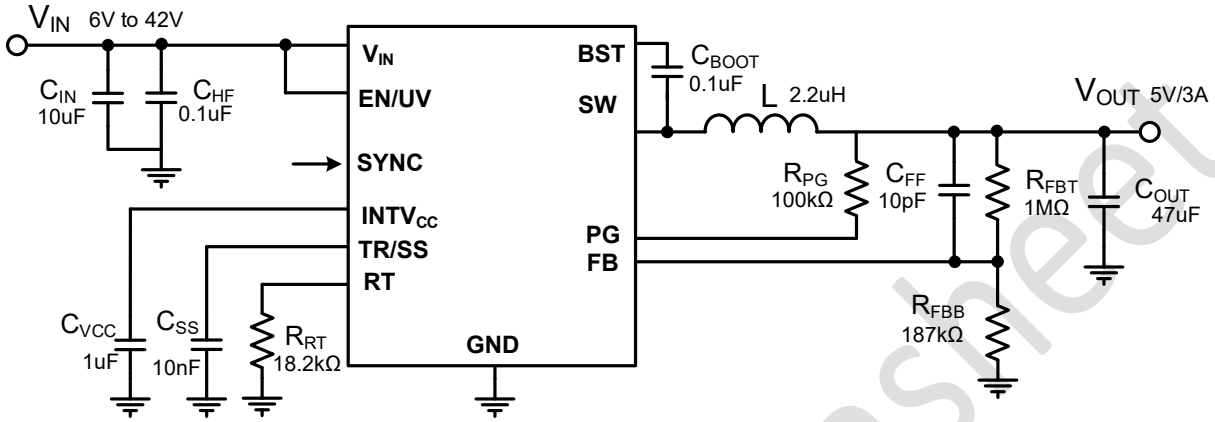


Fig.21 Typical Application Circuit (2MHz)

Table 2. Typical Parameter of Design

Parameter	Description
Input Voltage	V_{IN} = 6V to 42V
Output Voltage	V_{OUT} = 5V
Output Current	I_{OUT} = 3A
Switching Frequency	f_{SW} = 2MHz
Output Ripple	ΔV_{OUT_RIPPLE} = 10mV
Efficiency	92.5% at 1A from 12V_{IN} to 5V_{OUT}

Setting Output Voltage

The external feedback resistors connected to FB sets the output voltage. The feedback resistor values can be calculated with the below equation.

$$R_{FBB} = \frac{V_{REF} R_{FBT}}{V_{OUT} - V_{REF}}$$

While R_{FBT}=1MΩ, V_{REF}=0.782V, V_{OUT}=5V

Calculate R_{FBB}=187kΩ

Setting Switching Frequency

The AWK6809 uses a constant frequency PWM architecture which can be programmed to switch from 200kHz to 2.2MHz by connecting a resistor from R_T pin to ground. Table 2 gives typical R_T pin resistor R_T values for desired switching frequency. The R_T resistor required for the desired switching frequency can be calculated using:

$$R_T = \frac{49.6}{f_{sw}} - 5.4$$

Table 3. Frequency vs. R_T Value

fsw(kHz)	R_T(kΩ)
200	221
400	110
500	86.6
700	60.4
800	52.3
1000	40.2
1500	33.2
2000	18.2
2200	16.2

Inductor Selection

For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 20% to 40% of the maximum load current. The minimum inductance value can be calculated with the below equation.

$$L_M = \frac{V_{OUT}(1 - D)}{f_{SW} \times \Delta I_L}$$

While V_{OUT}=5V, f_{SW}=2000kHz, ΔI_L=30%×3A=0.9A, D=5V/12V=0.417

Calculate L_M=2.2μH.

Input Capacitor Selection

The input capacitor types can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (like X7R, C0G etc.) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. From the below equation, can easily calculate the input voltage ripple. Generally, required the input voltage ripple is less than 10% of the input voltage.

$$\Delta V_{IN} = \frac{I_O \times D \times (1 - D)}{f_{SW} \times C_{IN}}$$

Output Capacitor Selection

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with equation. Generally, required the output voltage ripple is less than 1% of the output voltage.

$$\Delta V_{OUT} = \frac{V_{OUT} \times (1 - D)}{8 \times {f_{SW}}^2 \times L \times C_{OUT}}$$

Bootstrap Capacitor Selection

A bootstrap capacitor connected between the BST pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the internal MOSFETs. A ceramic capacitor of 0.1uF and 16V voltage rating is required.

APPLICATION WAVEFORMS

Unless otherwise specified the following conditions apply: V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2MHz, L=2.2uH, C_{OUT} =44uF, T_J =25°C.

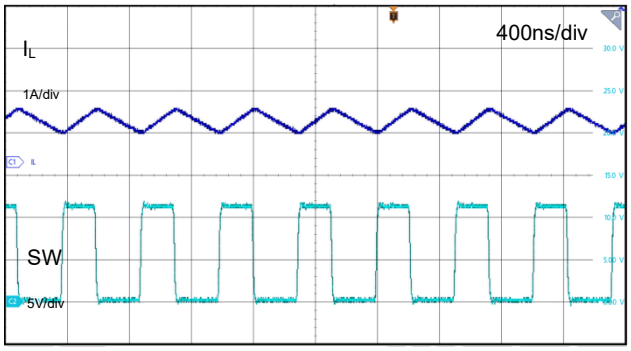


Fig.22 Steady State at I_{LOAD}=1A

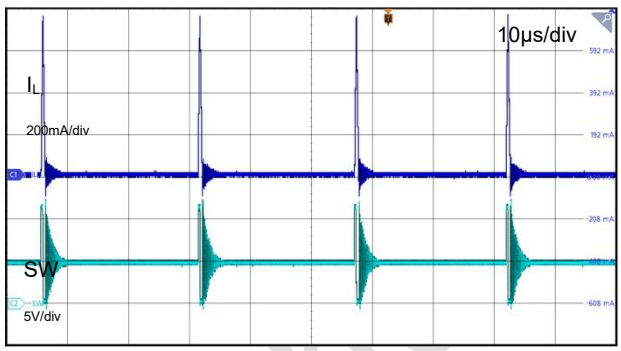


Fig.23 Steady State at I_{LOAD}=10mA, SYNC = 0V

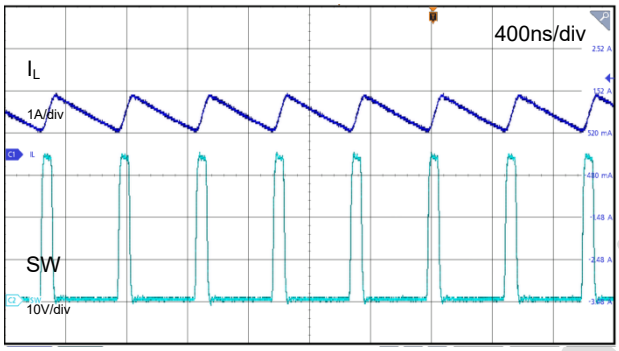


Fig.24 Steady State at V_{IN} = 36V, V_{OUT}= 5V, I_{LOAD}=1A

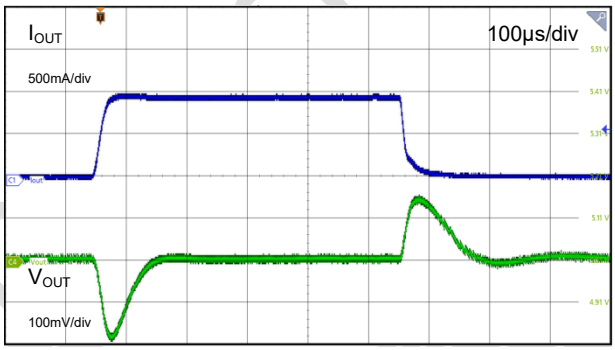


Fig.25 Load Transient at I_{LOAD} from 50mA to 1A

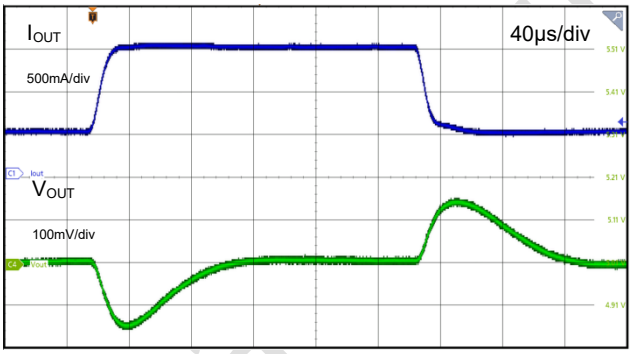


Fig.26 Load Transient at I_{LOAD} from 500mA to 1.5A

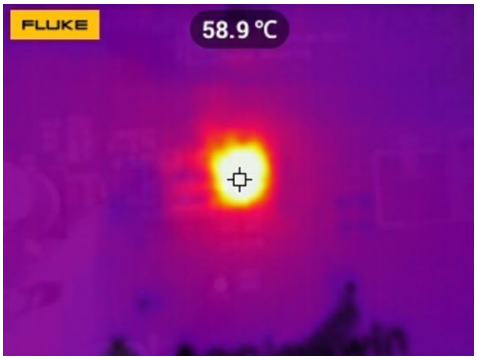


Fig.27 Thermal Performance at V_{OUT} = 5V, I_{LOAD} = 3A, f_{SW} = 2MHz

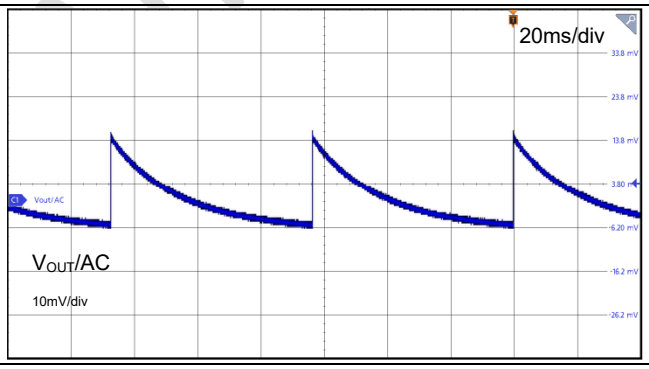


Fig.28 Output Ripple at I_{LOAD} =0A, Burst Mode Operation

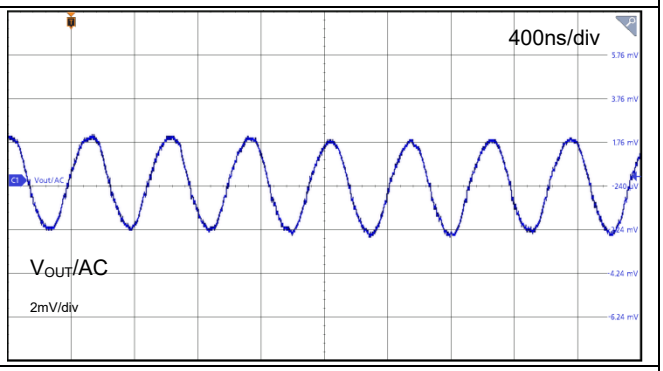


Fig.29 Output Ripple at I_{LOAD} =3A, Burst Mode Operation

PCB LAYOUT GUIDELINES

PCB layout is critical for stable operation of switching regulator AWK6809, especially for thermal design and EMI design. A four-layer layout is strongly recommended to achieve better thermal performance and EMI performance. For best results, please follow the guidelines below.

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible.

2. Make sure top switching loop with power have lowest impendence of grounding.

3. Use a large ground plane to connect to GND directly. And add vias near GND.

4. Output inductor should be placed close to the SW pin to minimize the SW area.

5. The FB terminal is sensitive to noise so the feedback resistor should be located as close as possible to the IC.

6. Keep the connection of the input capacitor and VIN as short and wide as possible.

From Fig.30 to Fig.33, there are some layout examples for reference.

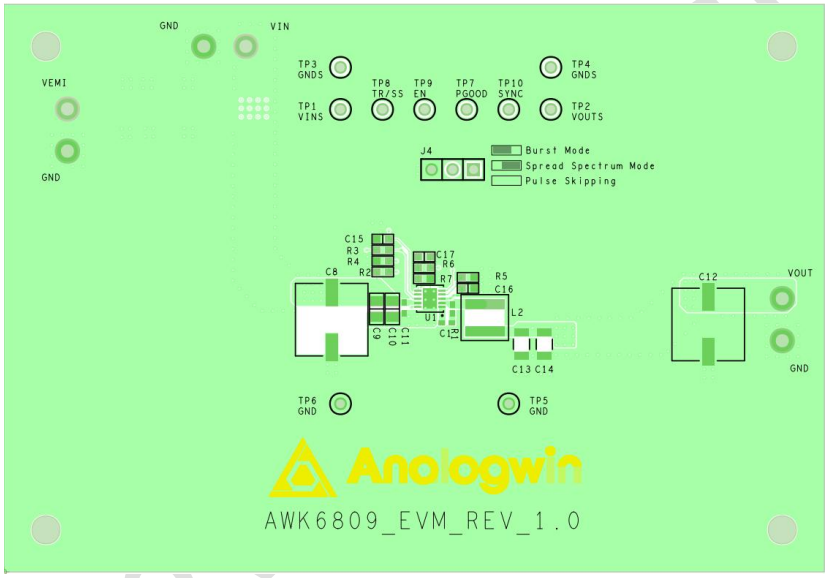


Fig.30 Top Layer

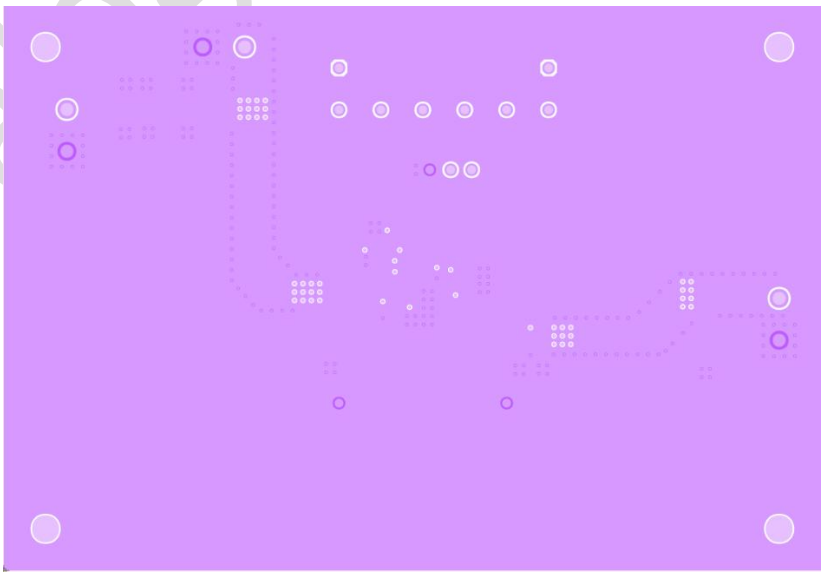


Fig.31 2nd Layer

Fig.32 3rd Layer

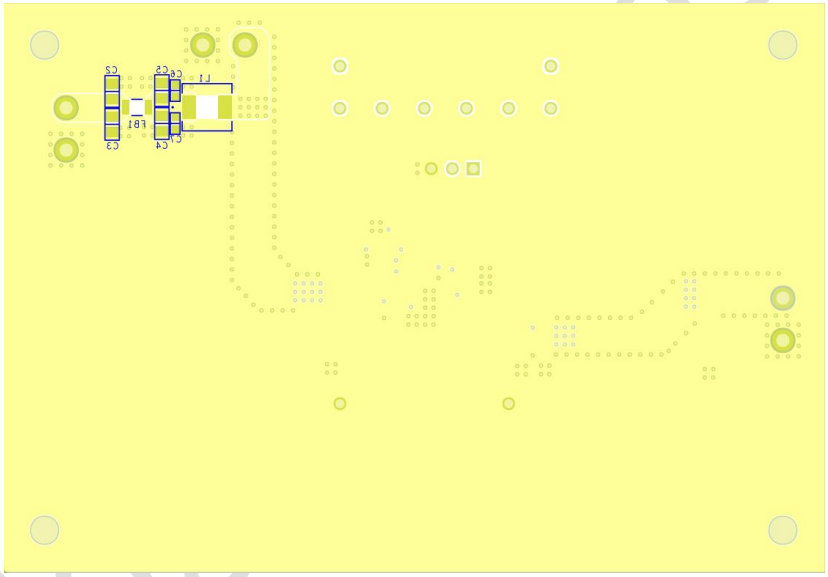


Fig.33 Bottom Layer

PACKAGE INFORMATION

Package Top marking

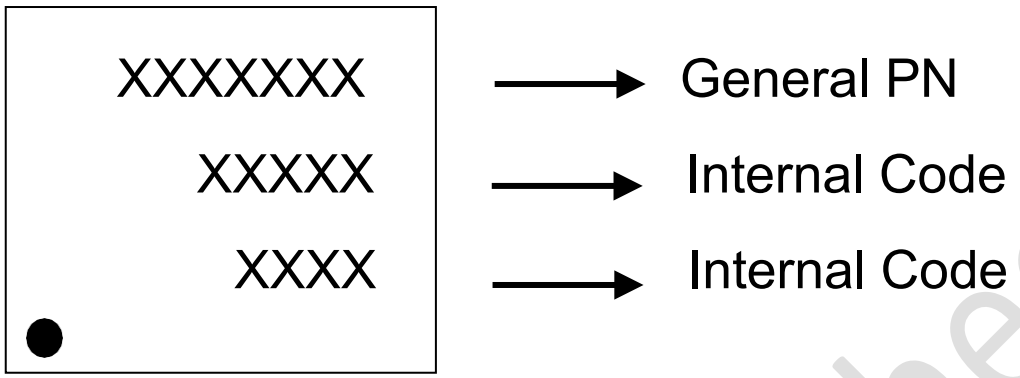


Fig.34 Package Top Marking

Tape and Reel Box Information

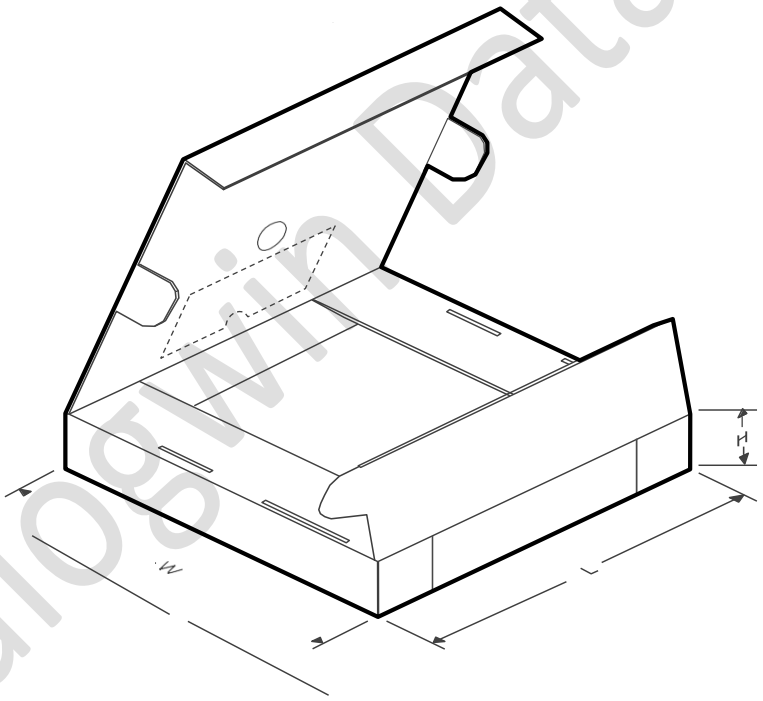


Fig.35 Tape and Reel Box Information

DEVICE	PACKAGE TYPE	PACKAGE DRAWING	PINS	SPQ	LENG (mm)	WIDTH (mm)	HEIGHT(mm)
AWK6809	DFN-10L	DD	10	3000	336.0	336.0	48.0
AWK6809	EMSOP-10L	LB	10	4000	336.0	336.0	48.0

Tape and Reel Information

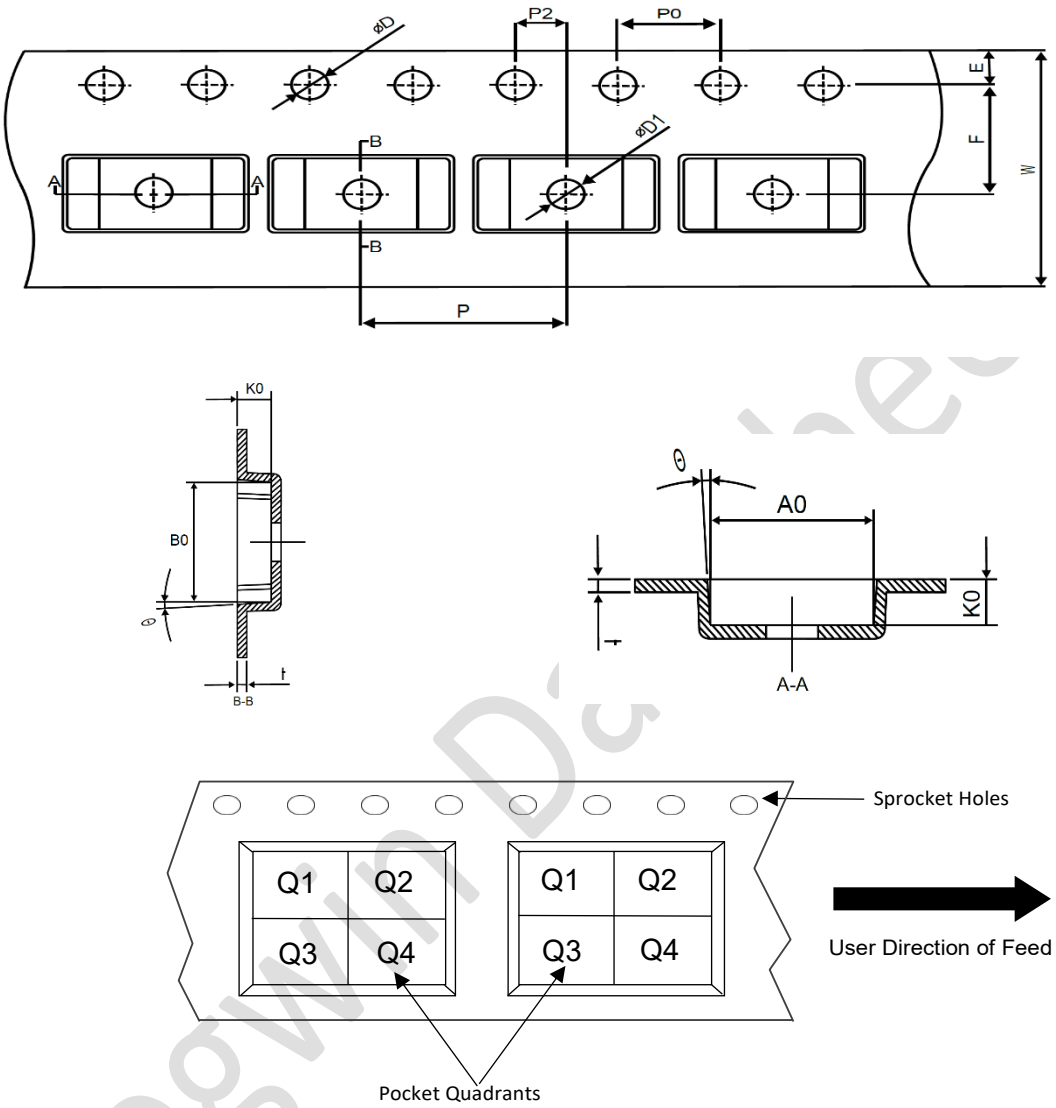


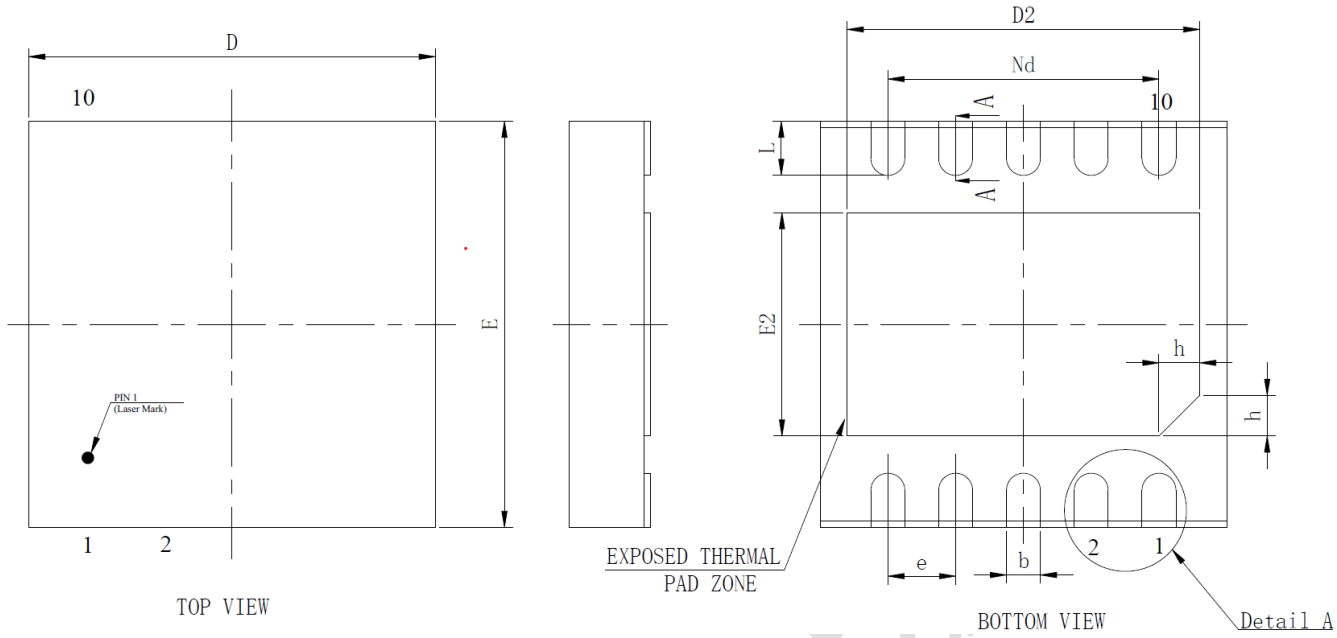
Fig.36 Tape and Reel Information

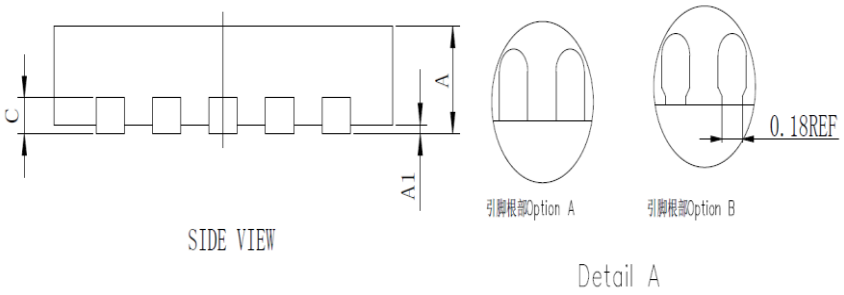
Device	Package Type	A0 (mm)	B0 (mm)	K0 (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant	Quantity
AWK6809DDR	DFN3X3-10L	3.30	3.30	1.10	8.00	4.00	12.00	Q1	3000
AWK6809LBR	EMSOP-10L	5.40	3.40	1.40	8.00	4.00	12.00	Q1	4000

DIMENSIONS AND PIN1 ORIENTATION

All dimensions are nominal

Package Outlines

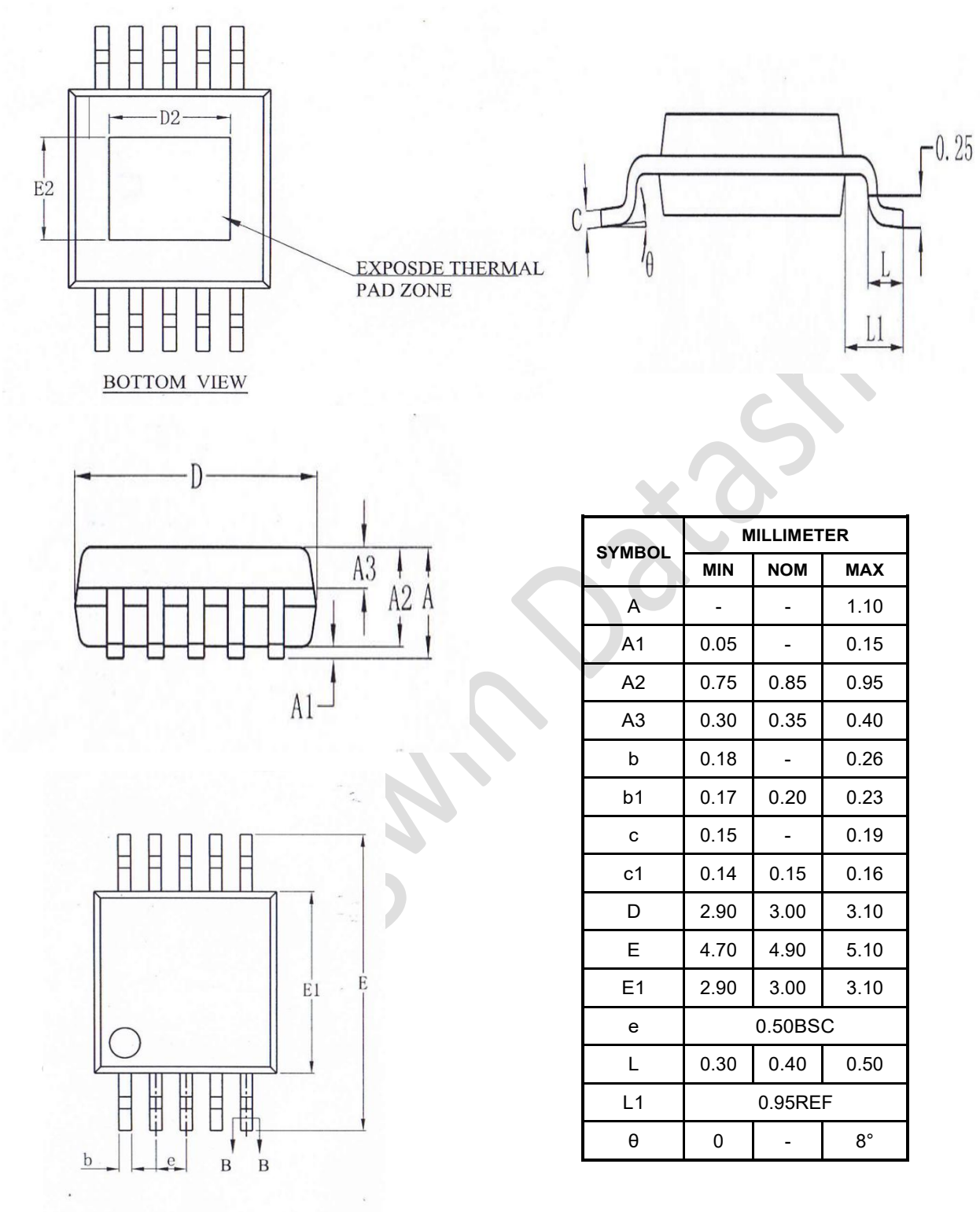




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1		0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e	0.50BSC		
Nd	2.00BSC		
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30

Fig.37 DFN3×3-10L Package, 3 mm × 3 mm Body

Package Outlines



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.10
A1	0.05	-	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.15	-	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.50BSC		
L	0.30	0.40	0.50
L1	0.95REF		
θ	0	-	8°

Fig.38 EMSOP-10L Package

ORDERING INFORMATION

Device	Order Part No.	Package	QTY
AWK6809	AWK6809DDR	DFN3x3-10L, Pb-Free	3000/Reel
	AWK6809LBR	EMSOP10L, Pb-Free	4000/Reel

REVISION HISTORY

DATE	REVISION	NOTES
March, 2025	1.0	Initial release
May,2025	1.1	1. Add EMOPS-10L package specifications. 2. The typical value of Sync High Input Voltage is changed from 2.7V to 2.85V. (Page 7)