Wide Input Voltage Range Boost/SEPIC/Flyback Converter with Random Spread Spectrum

AWT5157

FEATURES

- Wide Input Voltage of **2.9V to 45V**
- Low Operating Bias Current of **600μA** (Typ.)
- Programmable **100kHz** to **2.2MHz** Adjustable Switching Frequency
- Integrated Error Amplifier Allows Primary-side Regulation for Flyback Converter
- Selectable Random Spread Spectrum
- Input transient protection up to 50 V
- Low shutdown current **2μA** (Typ.)
- **48mΩ** R_{DSON} Switch
- PGOOD indicator
- 16-pin QFN package (3 mm × 3 mm)
- Selectable clock synchronization
- Programmable line UVLO
- Selectable **Hiccup** Overload Protection
- Over Voltage Protection
- Undervoltage Lockout with Hysteresis
- Thermal Shutdown
- Adjustable Soft Start

APPLICATION

- Battery-powered wide input boost, SPEIC, Flyback converter
- LED Bias Supply
- Portable Speaker Application
- Industrial PLC

DESCRIPTION

The AWT5157 is a non-synchronous boost converter with a wide input voltage range of 2.9V to 45V, the device can also be used in SEPIC and Flyback topologies.

The switching frequency can be programmed with an external resistor from 100kHz to 2.2MHz. Switching at 2.2MHz minimizes AM band interference, also allows a small solution size and a faster response. Besides, the AWT5157 offers selectable Random Spread Spectrum, which significantly improves the EMI performance.

The AWT5157 device has an internal 48mΩ R_{DSON} switch, together with low operating current and Pulse Frequency Modulation, high efficiency is guaranteed at both light and heavy load conditions.

The device has built-in protection features such as overvoltage protection, undervoltage lockout, thermal shutdown and optional Hiccup mode for overload protection. Additional features include programmable soft start, precision reference, power-good indicator, and external synchronization.

Device Information

DEVICE	PACKAGE	BODY SIZE(NOM)
AWT5157	QFN-16	3.00mm × 3.00mm

TYPICAL APPLICATION

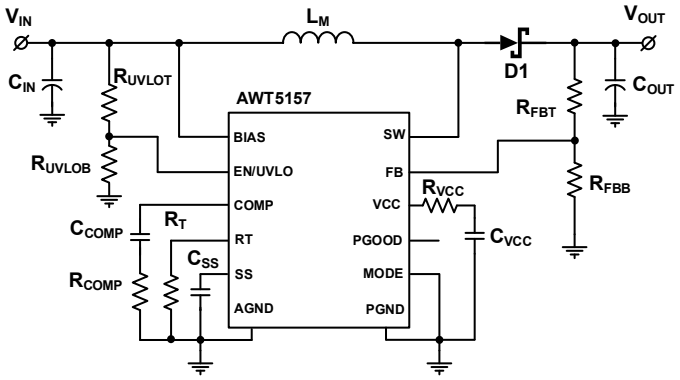

Fig.1 AWT5157 Typical (BOOST) Application

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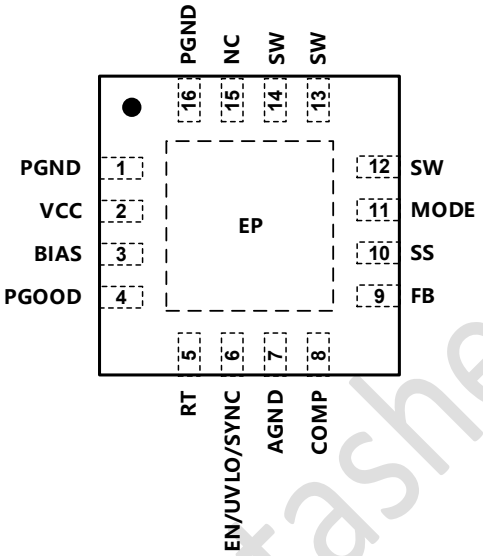
PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN16	

Pin Description

Table 1. AWT5157 Pin Description

No.	Pin	Type(1)	Description
1,16	PGND	G	Power Ground Pin
2	VCC	P	Output of Internal VCC Regulator, Connect a 1uF Ceramic Bypass Capacitor to PGND.
3	BIAS	P	Supply Voltage Input to the VCC Regulator, Connect a 100nF Ceramic Bypass Capacitor to PGND.
4	PGOOD	O	Power Good Pin
5	RT	I	Connect a Resistor to AGND to Program Switching Frequency.
6	EN/UVLO/SYNC	I	Enable, Undervoltage Lockout and External Synchronization Pin
7	AGND	G	Analog Ground Pin
8	COMP	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between this pin and AGND.
9	FB	I	Inverting input of the error amplifier. Connect a voltage divider to set the output voltage in boost, SEPIC, or primary-side regulated flyback topologies. Connect the low-side feedback resistor close to AGND.
10	SS	I	Connect a Capacitor to AGND to Program Soft Start Time.

No.	Pin	Type(1)	Description
11	MODE	I	Mode=0V or Connect to AGND, Hiccup Mode and Spread Spectrum are Both Disabled. Mode=285mV or Connect a 26.7kΩ Resistor to AGND, Hiccup Mode and Spread Spectrum are Both Enabled. Mode=600mV or Connect a 56.2kΩ Resistor to AGND, Hiccup Mode is Enabled and Spread Spectrum is Disabled. Mode>1V or Connect a 100kΩ Resistor to AGND, Hiccup Mode is Disabled and Spread Spectrum is Enabled.
12,13,14	SW		Switching Pin
15	NC	—	No Internal Connection
—	EP	—	Exposed Pad of Package

(1) G = Ground, I = Input, O = Output, P = Power

ABSOLUTE MAXIMUM RATINGS

Over the recommended operating junction temperature range(1)

		Min	Max	Units
Input	BIAS to AGND	-0.3	50	V
	EN to AGND	-0.3	50	
	SS, RT to AGND	-0.3	3.8	
	FB to AGND	-0.3	5	
	MODE to AGND	-0.3	3.8	
Output	VCC to AGND	-0.3	5.8	
	PGOOD to AGND	-0.3	22	
	SW to AGND	-0.3	47	
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

RECOMMENDED OPERATING CONDITIONS

		Min	Max	Units
Boost Regulator	V_{BIAS}	2.9	45	V
	V_{UVLO}	0	45	
	V_{FB}	0	4	
	f_{SW}	100	2200	kHz
Control	MODE	0	2	V
	PGOOD	0	20	V
T_J	Junction temperature	-40	150	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	Human body model (HBM)	±2000	V
	Charged device model (CDM)	±500	

ELECTRICAL CHARACTERISTICS

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{BIAS} = 12V, R_T = 9.09 kΩ. V_{OUT} is converter output voltage.

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Power Supply						
V_{BIAS}	BIAS UVLO threshold	V_{UVLO}=2V, Rising threshold	2.58	2.7	2.89	V
	BIAS UVLO hysteresis			160		mV
$I_{SHDN(BIAS)}$	BIAS shutdown current	V_{BIAS}=12V, V_{UVLO}=0V		2	5	μA
$I_{OPERATING(BIAS)}$	BIAS operating current	V_{BIAS}=12V, V_{UVLO}=2V, V_{FB}= V_{REF}, R_T=220kΩ		600	850	μA
VCC Regulator						
V_{CC_REG}	VCC Regulation	V_{BIAS}=12V, I_{VCC}=18mA	3.3	3.4	3.6	V
$V_{CC\_UVLO(RISING)}$	VCC UVLO threshold	VCC rising	2.3	2.5	2.75	V
	VCC UVLO hysteresis			140		mV
ENABLE						
$V_{EN(RISING)}$	Enable threshold	EN rising	0.5	0.8	1	V
$V_{EN(FALLING)}$	Enable threshold	EN falling	0.35	0.74	0.96	V
$V_{EN(HYS)}$	Enable hysteresis			65		mV
UVLO/SYNC						
$V_{UVLO(RISING)}$	UVLO/SYNC threshold	UVLO rising	1.42	1.5	1.59	V
$V_{UVLO(FALLING)}$	UVLO/SYNC threshold	UVLO falling	1.37	1.43	1.52	V
$V_{UVLO(HYS)}$	UVLO/SYNC threshold hysteresis			70		mV
I_{UVLO}	UVLO hysteresis current	V_{UVLO} =1.6V	3	5	7	μA
MODE, Spread Spectrum						
	F_{SW} modulation (upper limit)			8%		
	F_{SW} modulation (lower limit)			-8%		
Shutdown and Soft-Start						
I_{ss}	Internal Soft-Start Current		7.5	10	14	μA
	SS pulldown switch R_{DSON}			125		kΩ

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Current Limit						
I_{LIM}	Internal MOSFET current limit		6.5	8	9.5	A
Pulse Width Modulation						
fsw 1	Switching frequency	R_T =220 kΩ	84	105	130	kHz
fsw 2	Switching frequency	R_T =49.3 kΩ	395	450	505	kHz
fsw 3	Switching frequency	R_T =9.09 kΩ	1950	2200	2350	kHz
T_{ON_MIN}	Min. Turn On Time(1)	R_T =9.09 kΩ		80		ns
$D_{MAX\ 2}$	Maximum duty cycle limit(1)	R_T =220 kΩ		99%		
	R_T regulation voltage			0.5		V
Hiccup Mode Protection(1)						
	Hiccup Enable cycles			64		Cycles
	Hiccup timer reset cycles			8		Cycles
Error Amplifier						
V_{REF}	FB reference		0.98	1	1.02	V
Gm	Error Amplifier Transconductance	V_{COMP} =1.4V		2.5		mA/V
	COMP sourcing current	V_{COMP} =1.2 V	150			μA
	COMP clamp voltage	COMP falling		0.75	1	V
A_{CS}	ΔV_{COMP} / ΔI_{SW}			0.079		
OVP						
V_{OVTH}	Overvoltage threshold	FB rising (reference to V_{REF})	107%	110%	113%	
	Overvoltage threshold	FB falling (reference to V_{REF})		106%		
Thermal Shutdown						
T_{SD}	Thermal Shutdown threshold	Temperature rising		165		°C
T_{HYS}	Thermal Shutdown hysteresis			10		°C

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PGOOD						
	PGOOD pulldown switch R_{DSON}	1mA sinking		65		Ω
V_{UVTH}	Undervoltage threshold	FB rising (reference to V_{REF})		94%		
	Undervoltage threshold	FB falling (reference to V_{REF})	87%	90%	93%	
Power Switch						
$R_{DS(ON)}$	Internal MOSFET on-resistance	V_{BIAS}=12V		48	110	mΩ
	Leakage current	V_{SW}=12V			3000	nA

(1) Derived from bench characterization. Not tested in production.

FUNCTIONAL DIAGRAM

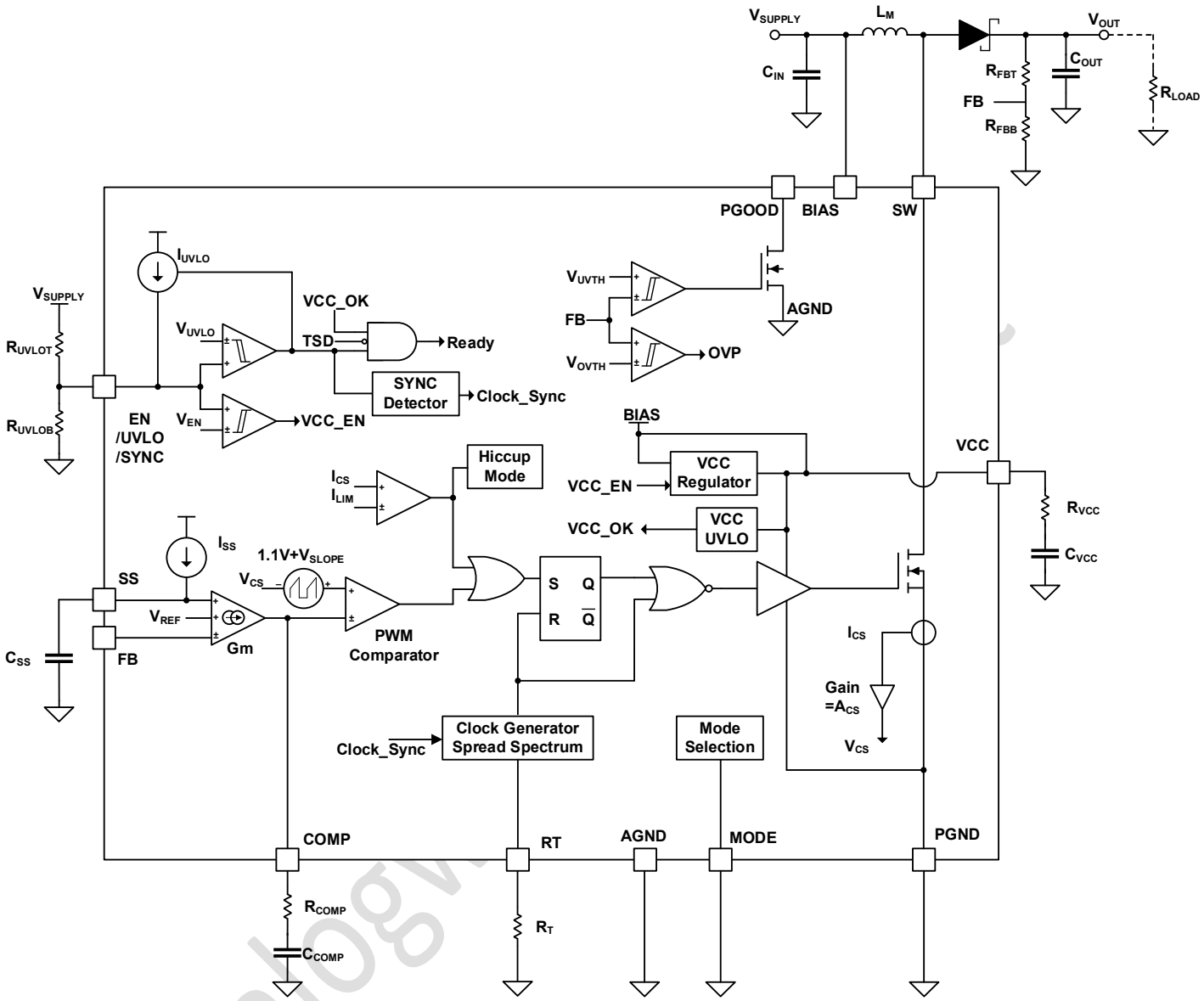


Fig.2 Diagram Block

TYPICAL CHARACTERISTICS

Unless otherwise specified the following conditions apply: V_{BIAS} =12V, f_{SW} =2MHz, L=1.5uH, T_J =25°C

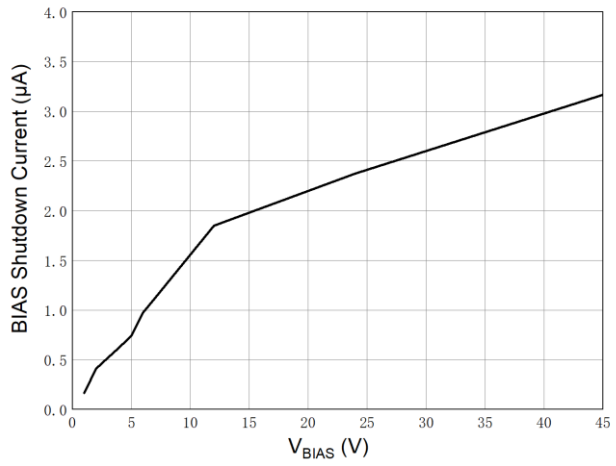


Fig.3 BIAS Shutdown Current vs. V_{BIAS}

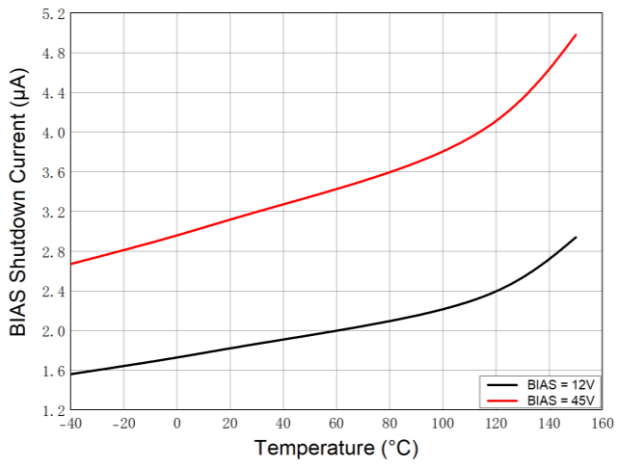


Fig.4 BIAS Shutdown Current vs. Temperature

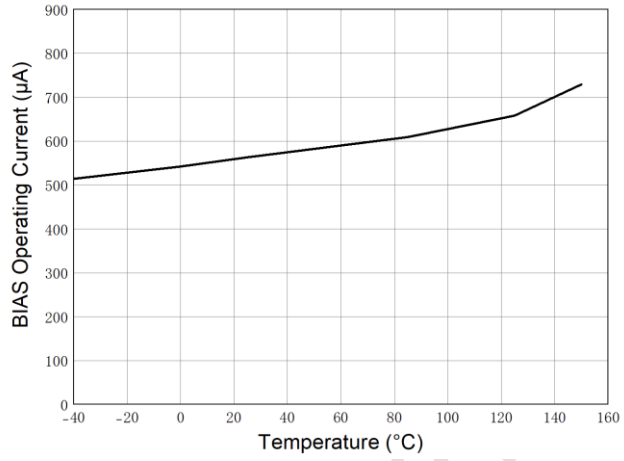


Fig.5 BIAS Operating Current vs. Temperature

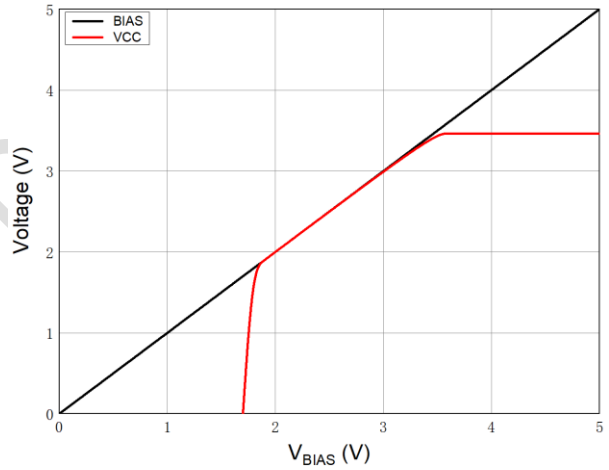


Fig.6 V_{VCC} vs. V_{BIAS}

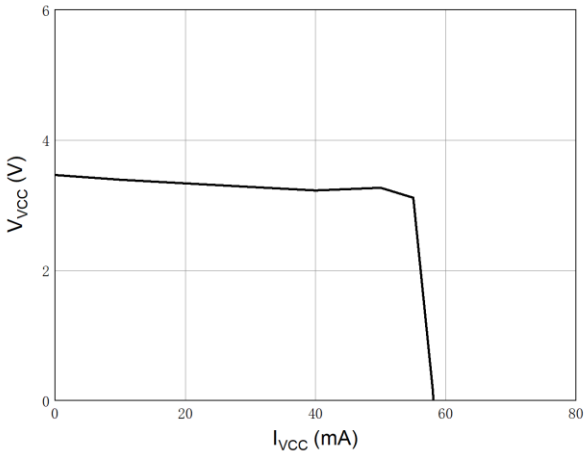


Fig.7 V_{VCC} vs. I_{VCC}

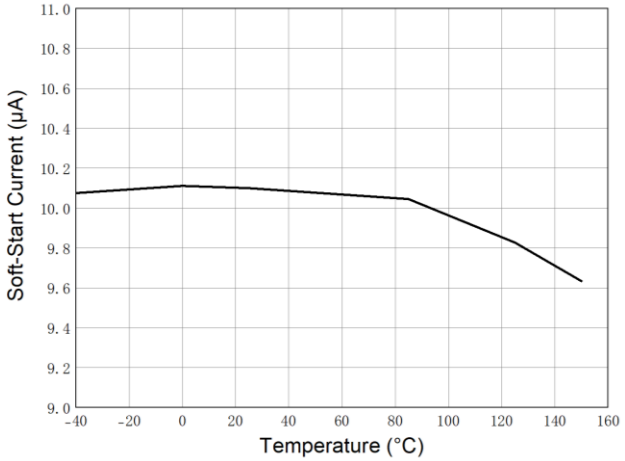


Fig.8 I_{SS} vs. Temperature

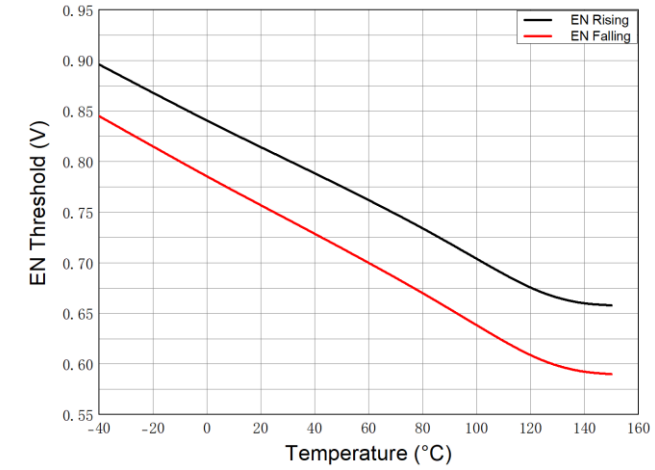


Fig.9 EN Threshold vs. Temperature

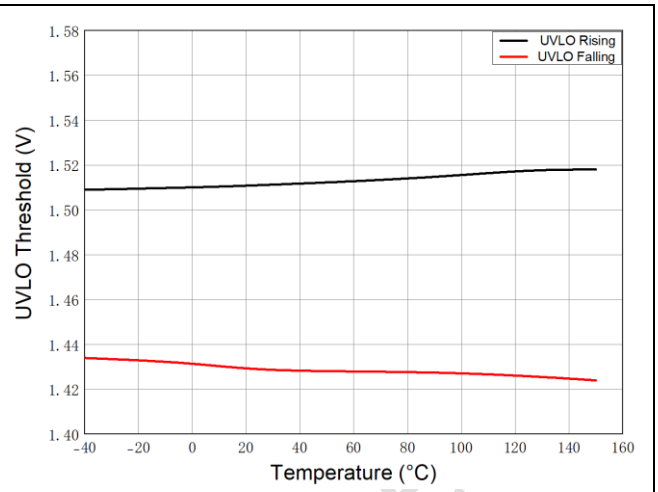


Fig.10 UVLO Threshold vs. Temperature

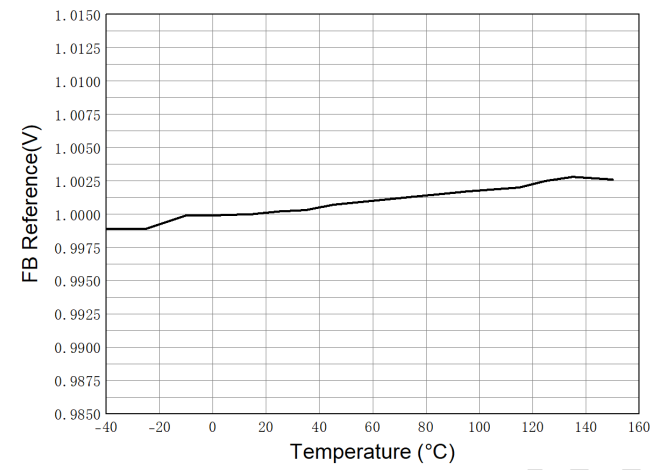


Fig.11 FB Reference vs. Temperature

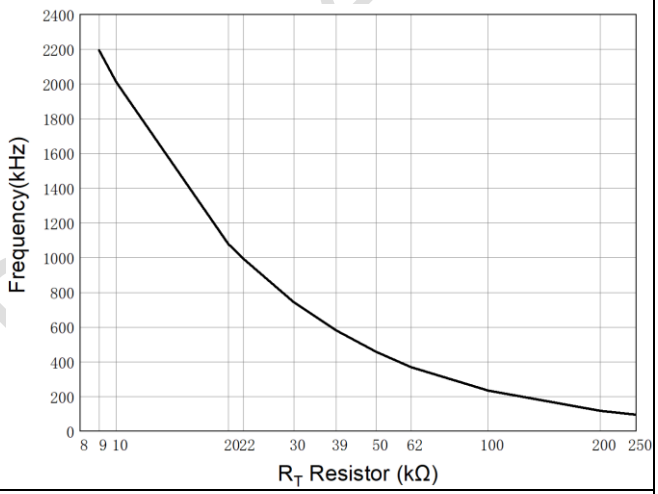


Fig.12 Frequency vs. R_T Resistance

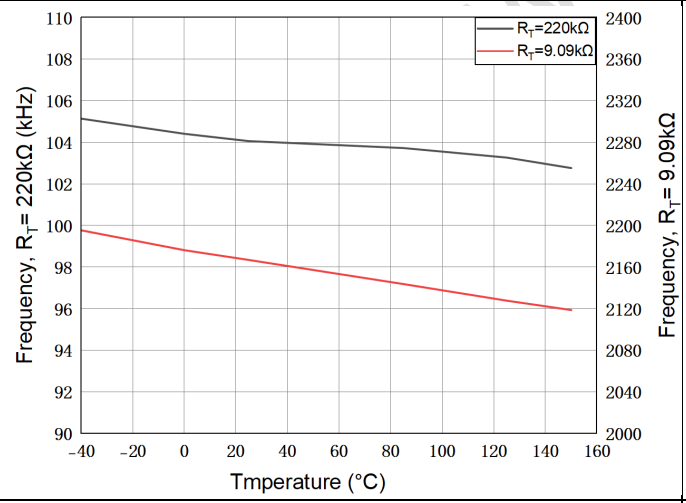


Fig.13 Frequency vs. Temperature

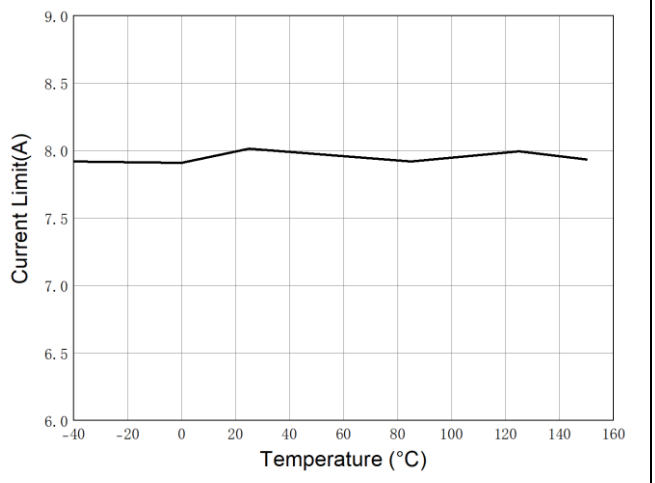


Fig.14 Current Limit vs. Temperature

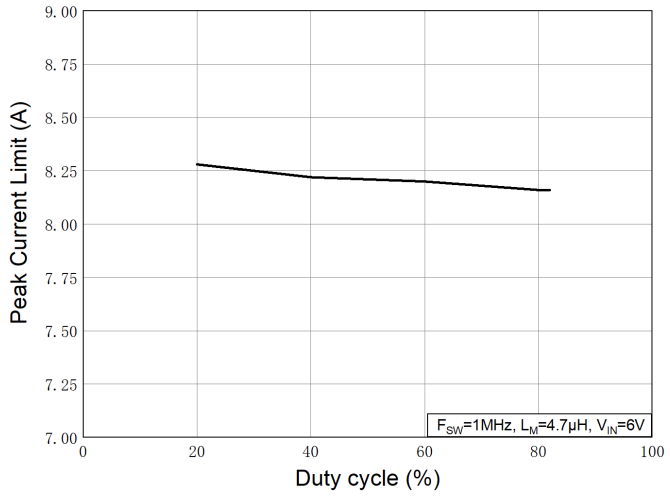


Fig.15 Peak Current Limit vs. Duty Cycle

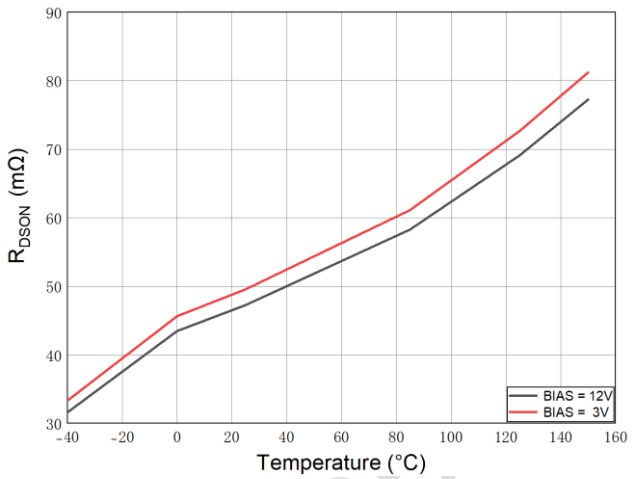


Fig.16 Internal MOSFET Drain Source On-state Resistance vs. Temperature

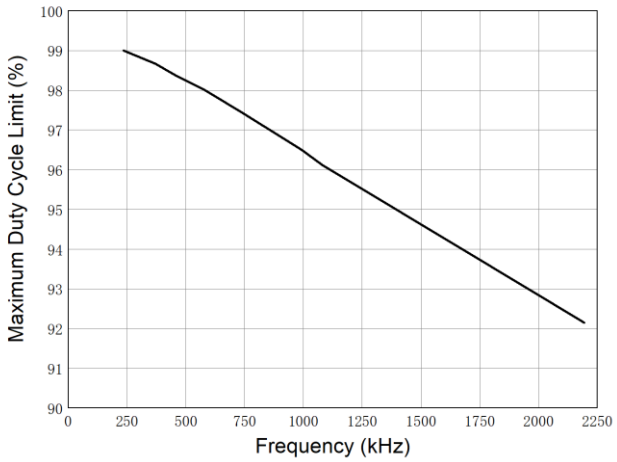


Fig.17 Maximum Duty Cycle Limit vs. Frequency

PRODUCT OVERVIEW

The AWT5157 is a wide input range, non-synchronous boost converter that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies. It can start up from a single-cell battery with a minimum voltage of 2.9V. The internal VCC regulator also supports BIAS pin operation up to 45 V. The switching frequency is dynamically programmable with an external resistor from 100kHz to 2.2MHz. Switching at 2.2MHz minimizes AM band interference and allows for a small solution size and fast transient response. The device provides an optional random spread spectrum, which significantly improves the EMI performance.

Random Spread Spectrum

The AWT5157 provides a spread spectrum, which reduces the EMI of the power supply over a wide frequency range with a typical upper and lower limit of ± 8% for FSW modulation. This function is enabled by a single resistor (26.7 kΩ or 100 kΩ) between the MODE pin and the AGND pin or by programming the MODE pin voltage (285 mV or greater than 1.0 V) during initial power up. When the spread spectrum is enabled, it can effectively optimize EMI interference.

Hiccup Mode Overload Protection (MODE Pin)

The AWT5157 provides selectable Hiccup mode overload protection. This function is enabled by a single resistor (26.7 kΩ or 56.2 kΩ) between the MODE pin and the AGND pin or by programming the MODE pin voltage (285 mV or 600 mV) during initial power up. The internal Hiccup mode fault timer of the device counts the PWM clock cycles when the cycle-by-cycle current limiting occurs after soft start is finished. When the Hiccup mode fault timer detects 64 cycles of current limiting, an internal Hiccup mode off timer forces the device to stop switching and pulls down SS. Then, the device restarts after 16ms of Hiccup mode off time. The 64-cycle Hiccup mode fault timer is reset if eight consecutive switching cycles occur without exceeding the current limit threshold. The soft-start time must be long enough not to trigger the Hiccup mode protection after the soft start is finished.
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Line Undervoltage Lockout (UVLO/SYNC/EN Pin)

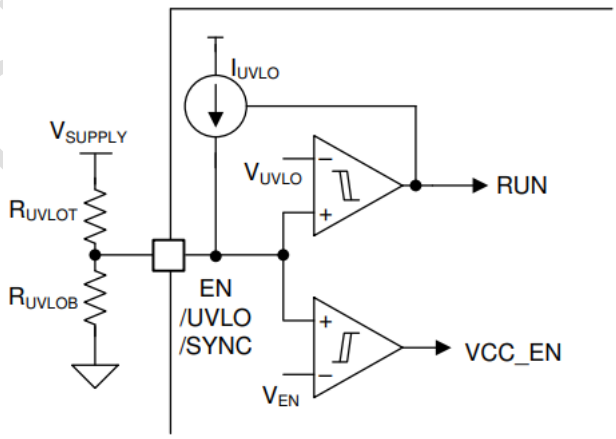


Fig.18 Line Undervoltage Lockout diagram

The AWT5157 has a dual-level EN/UVLO circuit. During power on, if the BIAS pin voltage is greater than 2.9 V and the UVLO pin voltage is between the enable threshold (V_{EN}) and the UVLO threshold (V_{UVLO}) for more than 1.5 µs the device starts up and an internal configuration starts. When the UVLO pin voltage is above the UVLO threshold, the device enters Run mode. In Run mode, a soft start

sequence starts if the VCC voltage is greater than the VCC UV threshold ($V_{VCC-UVLO}$). UVLO hysteresis is accomplished with an internal 70 mV voltage hysteresis and an additional 5 μA current source that is switched on or off. When the UVLO pin voltage exceeds the UVLO threshold, the UVLO hysteresis current source is enabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the UVLO threshold, the current source is disabled, causing the voltage at the UVLO pin to fall quickly. When the UVLO pin voltage is less than the enable threshold (V_{EN}), the device enters Shutdown mode after a 40 μs (typical) delay with all functions disabled.

Clock Synchronization (UVLO/SYNC/EN Pin)

The AWT5157 switching frequency can be synchronized to an external clock by pulling down the EN/UVLO/SYNC pin. The internal clock of the device is synchronized at the falling edge. The duty cycle of the pulldown pulse is greater than 20%. And the minimum pulldown pulse width must be greater than 150 ns, the duty cycle of the pullup pulse is greater than 20%. And the minimum pullup pulse width must be greater than 150 ns. The external clock frequency (f_{SYNC}) must be within +25% and –30% of $f_{RT(typical)}$.

Overvoltage Protection (OVP)

The AWT5157 has OVP for the output voltage. OVP is sensed at the FB pin. If the voltage at the FB pin rises above the overvoltage threshold (V_{OVTH}), OVP is triggered and switching stops. During OVP, the internal error amplifier is operational.

Thermal Shutdown (TSD)

An internal thermal shutdown disables switching, and pulls down the SS when the junction temperature exceeds the thermal shutdown threshold (T_{TSD}). When the temperature drops to the TSD recovery temperature, the device performs a soft start.

Power Good Indicator (PGOOD Pin)

The device has a Power-Good indicator (PGOOD) to simplify sequencing and supervision. The PGOOD switches to a high impedance open-drain state when the FB pin voltage is greater than the feedback undervoltage threshold (V_{UVTH}), the VCC is greater than the VCC UVLO threshold and the UVLO/EN is greater than the EN threshold. A 25 μs deglitch filter prevents any false pulldown of the PGOOD due to transients. The recommended minimum pullup resistor value is 10 kΩ.

APPLICATION INFORMATION

Fig.19 shows all optional components to design a boost converter.

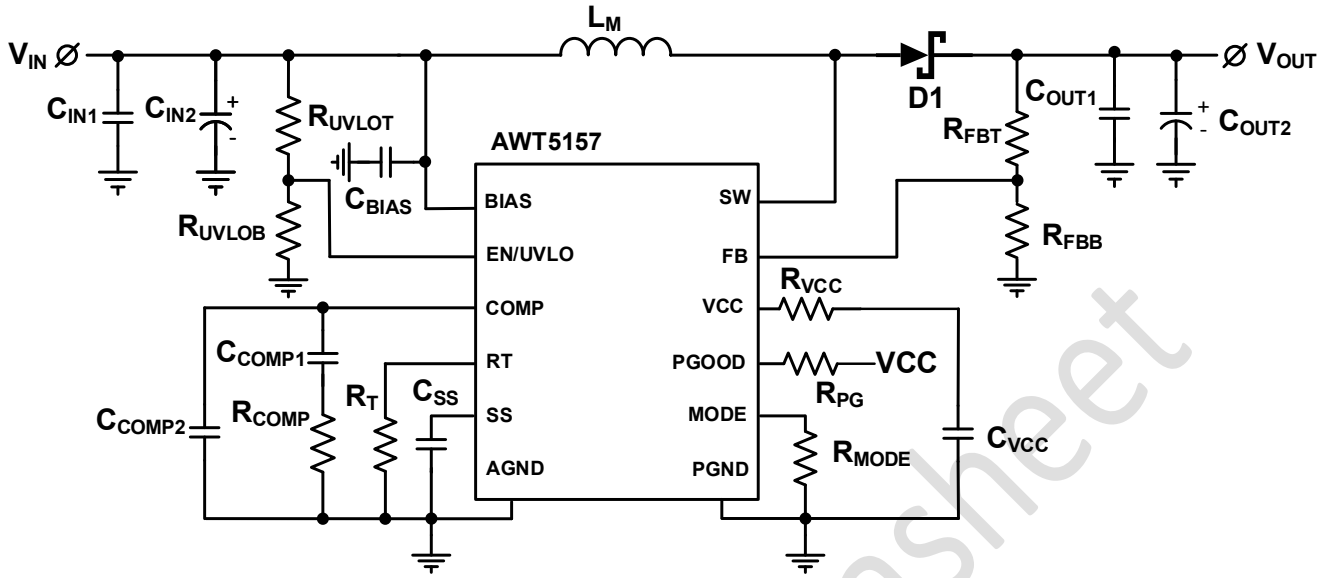


Fig.19 Typical Boost Converter Circuit

Table 2. shows the intended input, output, and performance parameters for this application example.

Table 2. Typical Parameter of Design

Parameter	Description
Input Voltage Range	V_{IN} = 2.9V to 9V
Output Voltage	V_{OUT} = 12V
Output Current	I_{OUT} = 1.6A
Switching Frequency	f_{SW} = 2MHz
Efficiency	> 91% at V_{IN}=6V, I_{OUT} =1A

Setting Output Voltage

The external feedback resistors connected to FB sets the output voltage. The feedback resistor values can be calculated with the below equation.

$$R_{FBB} = \frac{V_{REF} R_{FBT}}{V_{OUT} - V_{REF}} \quad (1)$$

While R_{FBT}=50kΩ, V_{REF}=1.0V, V_{OUT}=12V

Calculate R_{FBB}≈4.53kΩ

Setting Switching Frequency

The switching frequency of the AWT5157 can be programmed from 100kHz to 2.2MHz by connecting a resistor from R_T pin to ground. Table 2 gives typical R_T pin resistor R_T values for desired switching frequency. The R_T resistor required for the desired switching frequency can be calculated using:

$$R_T = \frac{23722}{f_{SW}} - 1.7 \quad (2)$$

While f_{SW}=2200kHz, Calculate R_T≈9.09kΩ

Table 3. Frequency VS. R_T Value

fsw(kHz)	R_T(kΩ)
105	220
450	49.3
2000	9.53
2200	9.09

Inductor Selection

For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can be calculated with the below equation.

$$L_M = \frac{V_{IN} \times D}{f_{SW} \times \Delta I_L} \quad (3)$$

While V_{IN} = 5V, V_{OUT} = 12V, f_{SW} = 2000kHz, D = (12-5)/12 ≈ 0.583, ΔI_L = 0.3*1.5/(1-0.583)=1.08A

Calculate L_M ≈1.5uH.

Input Capacitor Selection

The input capacitor types can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (like X7R, C0G etc.) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. From the below equation, can easily calculate the input voltage ripple. Generally, required the input voltage ripple is less than 10% of the input voltage.

$$\Delta V_{IN} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{IN}} \quad (4)$$

Output Capacitor Selection

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with equation. Generally, required the output voltage ripple is less than 1% of the output voltage.

$$\Delta V_{OUT} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{f_{SW} \times C_{OUT}} \quad (5)$$

UVLO Resistor Selection

The external UVLO resistor divider must be designed so that the voltage at the UVLO pin is greater than 1.5V (typical) when the input voltage is in the desired operating range. The values of R_{UVLOT} and R_{UVLOB} can be calculated as shown in Equation 6 and Equation 7.

$$R_{UVLOT} = \frac{V_{SUPPLY(ON)} \cdot \frac{V_{UVLO(FALLING)}}{V_{UVLO(RISING)}} - V_{SUPPLY(OFF)}}{I_{UVLO}} \quad (6)$$

where

•$V_{SUPPLY(ON)}$ is the desired start-up voltage of the converter

•$V_{SUPPLY(OFF)}$ is the desired turn-off voltage of the converter

Using Equation 7, the bottom UVLO resistor (R_{UVLOB}) is calculated.

$$R_{UVLOB} = \frac{V_{UVLO(RISING)} \cdot R_{UVLOT}}{V_{SUPPLY(ON)} - V_{UVLO(RISING)}} \quad (7)$$

Soft-Start Capacitor Selection

The soft-start capacitor is used to control the overshoot of the load voltage and inrush current during the start-up of the regulator. Equation 8 is used to calculate the minimum recommended soft-start capacitor value.

$$C_{SS} = \frac{I_{SS} \cdot V_{OUT} \cdot C_{OUT2}}{I_{LOAD}} \quad (8)$$

Feedback Resistor Selection

The feedback resistors (R_{FBT}, R_{FBB}) determines the regulated output voltage. To help limit the bias current of the feedback resistor divider. Equation 9 is used to calculate the value of R_{FBB}.

$$R_{FBB} = \frac{R_{FBT}}{\frac{V_{OUT}}{V_{REF}} - 1} \quad (9)$$

Crossover Frequency (f_{cross}) Selection

The crossover frequency of the loop can be either selected to be 1/10 the switching frequency or 1/5 the right-half plane zero frequency, whichever is lower. Equation 10 shows the calculation for 1/10 the switching frequency. Equation 11 show how to calculate the 1/5 the right half plane zero frequency at full load condition.

$$f_{CROSS} = \frac{f_{sw}}{10} \quad (10)$$

$$f_{CROSS\_1} = \frac{f_{Z\_RHP}}{5} = \frac{R_{LOAD} \cdot D'^2}{5 \cdot 2 \cdot \pi \cdot L_M} \quad (11)$$

where

• D' is (1 -D) the minimum supply voltage
• R_{LOAD} is the load resistance equal to V_{OUT} / I_{LOAD}

R_{COMP} Selection

The R_{COMP} value directly affects the crossover frequency of the control loop. R_{COMP} is calculated using Equation 12.

$$R_{COMP} = \frac{2\pi \cdot C_{OUT2} \cdot A_{CS} \cdot V_{OUT}^2 \cdot f_{CROSS}}{g_m \cdot V_{IN\_min}} \quad (12)$$

where

• gm is the transconductance of the error amplifier.
• ACS is the equivalent current sensing gain.

C_{COMP1} Selection

The R_{COMP} resistor and C_{COMP1} capacitor set the low frequency zero of the compensation network. C_{COMP1} is calculated using Equation 13.

$$C_{COMP1} = \sqrt{\frac{C_{OUT} \cdot R_{LOAD}}{4\pi \cdot R_{COMP}^2 \cdot f_{CROSS}}} \quad (13)$$

C_{COMP2} Selection

The C_{COMP2} capacitor sets the high frequency pole of the compensation network. The high frequency pole aids in attenuating high frequency noise due to the switching frequency and assuring enough gain margin. Equation 14 is used to calculate the value of C_{COMP2}.

$$C_{COMP2} = \frac{C_{COMP1} \cdot L_M}{C_{COMP1} \cdot D'^2 \cdot R_{LOAD} \cdot R_{COMP} - L_M} \quad (14)$$

Diode Selection

A Schottky is the preferred type for a D1 diode due to its low forward voltage drop and small reverse recovery charge. When choosing Schottky diodes, low reverse leakage current is an important parameter. It must be able to handle the average output current.

Application Curve

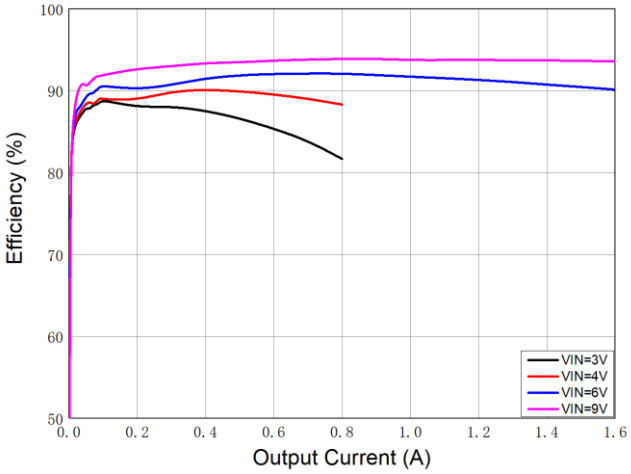


Fig.20 Efficiency versus Output Current

PCB LAYOUT GUIDELINES

PCB layout is critical for stable operation of switching regulator AWT5157, especially for thermal design and EMI design. For best results, please refer to Fig. 21 and follow the guidelines below.

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible.
2. Make sure top switching loop with power have lowest impendence of grounding.
3. Leave a copper area near the D1 diode for thermal dissipation.
4. Use a large ground plane to connect to GND directly. And add vias near GND.
5. Output inductor should be placed close to the SW pin to minimize the SW area.
6. The FB terminal is sensitive to noise so the feedback resistor should be located as close as possible to the IC.
7. Keep the connection of the input capacitor and VIN as short and wide as possible.
8. For more device applications, please refer to the related Evaluation Board User's Guide.

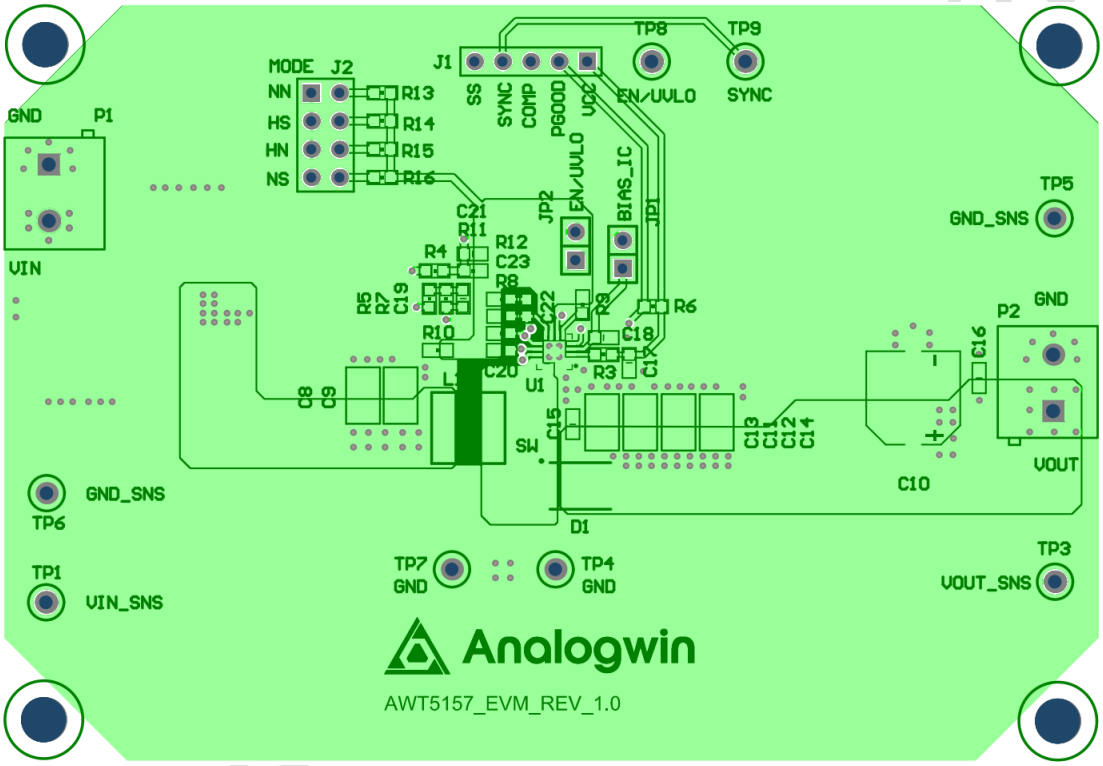


Fig.21 Layout Example

PACKAGE INFORMATION

Package Top marking

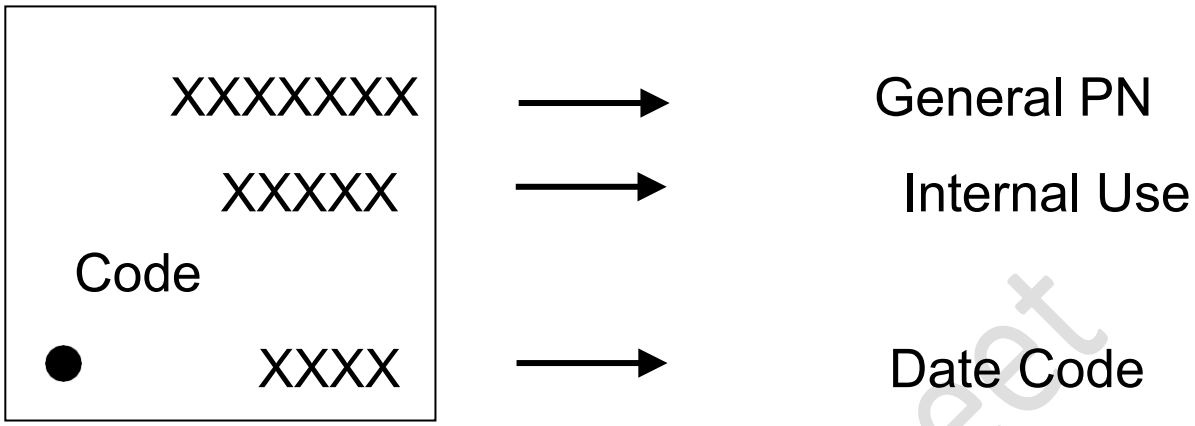


Fig.22 Package Top Marking

Tape and Reel Box Information

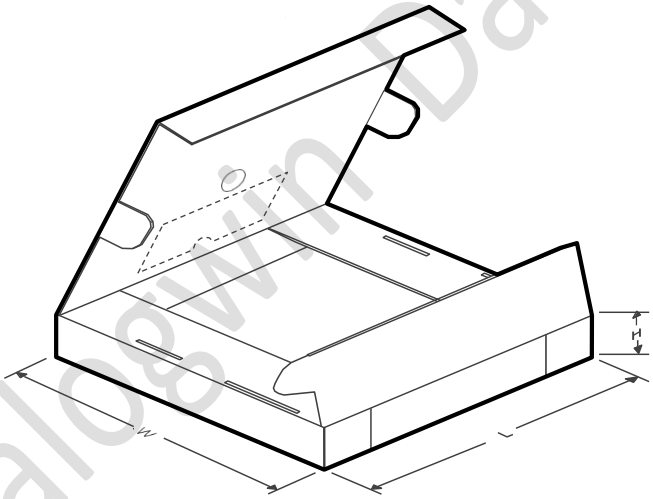


Fig.23 Tape and Reel Box Information

DEVICE	PACKAGE TYPE	PACKAGE DRAWING	PINS	SPQ	LENG (mm)	WIDTH (mm)	HEIGHT(mm)
AWT6722	QFN-16	BE	16	3000	320.0	320.0	48.0

Tape and Reel Information

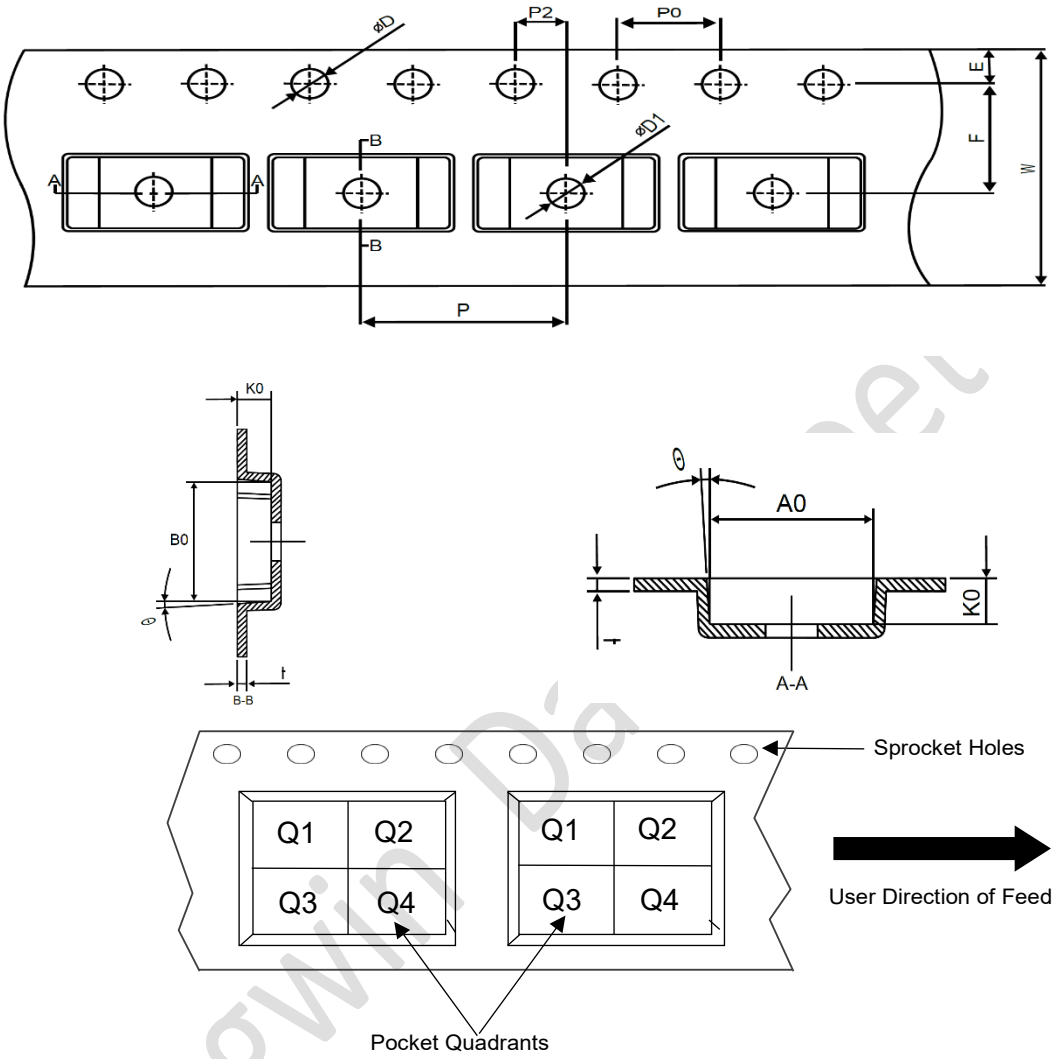


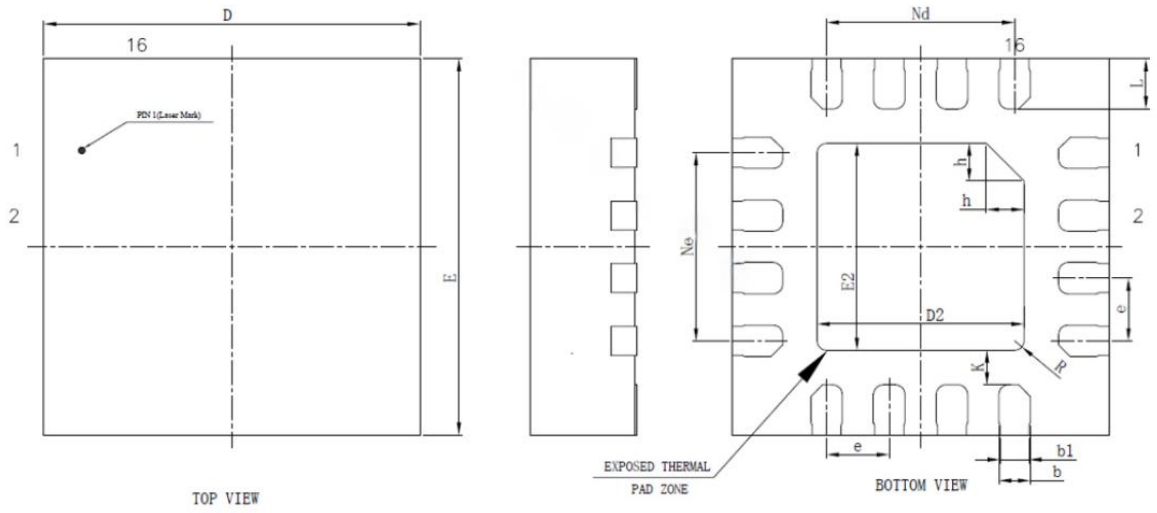
Fig.24 TAPE and Reel Information

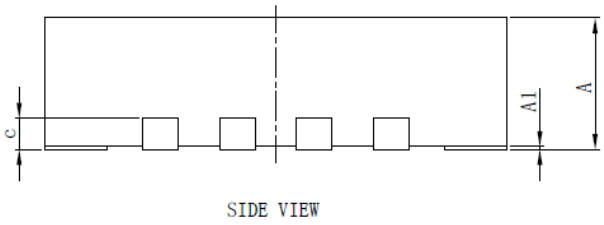
DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	A0 (mm)	B0 (mm)	K0 (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant	Quantity
AWT5157	QFN-16	3.30	3.30	1.10	8.00	4.00	12.00	Q1	3000

All dimensions are nominal

Package Outlines





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1		0.02	0.05
b	0.20	0.25	0.30
b1	0.23REF		
c	0.203REF		
D	2.90	3.00	3.10
D2	1.60	1.65	1.70
e	0.50BSC		
Nd	1.50BSC		
Ne	1.50BSC		
E	2.90	3.00	3.10
E2	1.60	1.65	1.70
L	0.35	0.40	0.45
h	0.25	0.30	0.35
K	0.225	0.275	0.325
R	0.075REF		

Fig.25 QFN3×3-16L Package, 3 mm × 3 mm Body

ORDERING INFORMATION

Device	Order Part No.	Package	QTY
AWT5157	AWT5157BER	QFN3x3-16L, Pb-Free	3000/Reel

REVISION HISTORY

DATE	REVISION	NOTES
Jan. 2025	1.0	Initial release