60V, 3A, High-Efficiency, Compact, Fully Integrated, Synchronous Buck Converter

AWK4573

KEY FEATURES

- Wide Input range: 3.4V to 60V
- 3A Continuous Output Current
- High-Efficiency, Synchronous Mode Control
- 230mΩ/50mΩ Internal Power MOSFETs
- Adjustable Switching Frequency: 300kHz to 2.2MHz
- 180° Out-of-Phase SYNCO Clock
- Low 30μA Operating Quiescent Current From $24V_{IN}$ to $5V_{OUT}$
- Low 1.5μA Shutdown Current
- FB Voltage Tolerance: 0.8V ±2% over the Full Temperature Range (–40°C to +125°C)
- Selectable Pulse Frequency Modulation (PFM) Mode or Forced Continuous Conduction Mode (FCCM) during Light-Load Operation
- Precision Enable and Power Good (PG)
- Output 0.7ms Soft-Start
- Low-Dropout (LDO) Mode Operation
- V_{IN} Under-Voltage Lockout (UVLO)
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup mode
- Thermal Shutdown
- Available in a QFN-12 (2.5mmx3mm) Package

APPLICATIONS

- Telecommunications Infrastructure
- Lamps and LEDs
- Motor Controls
- Industrial Power Systems
- IoT sensor

GENERAL DESCRIPTION

The AWK4573 is a 3A synchronous step-down, DC-DC converter, which integrated a 230mΩ high-side MOSFET and a 50mΩ low-side MOSFET to provide a high efficiency solution.

The AWK4573 provides a wide input range, from 3.4V to 60V, which is highly adaptable to a wide variety of step-down applications within Industrial and telecom environments. With a shutdown current as low as 1.5μA, this device is also an ideal option for battery-powered applications.

The AWK4573 uses peak-current-mode control (with the integrated compensation), Pulse Frequency Modulation (PFM) mode scheme for excellent stability, output accuracy and transient response.

Implemented Internally, soft-start function and slope compensation circuits reduces design time and allows the device to be used with the minimum the external components. The support for a close-to-100% duty cycle and Low-Dropout (LDO) Mode operation enables the device to withstand automotive cold cranking.

The AWK4573 features power good function, undervoltage lockout (UVLO), cycle-by-cycle over-current protection, hiccup mode short-circuit protection, thermal shutdown.

This device is available in a compact, 12-lead, 2.5mm × 3mm QFN package.

TYPICAL APPLICATION

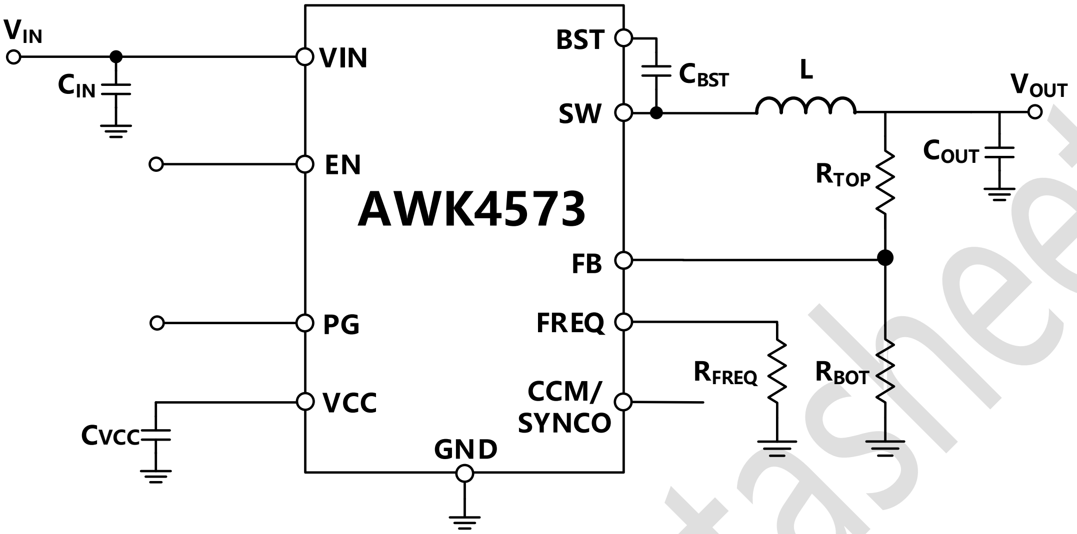

Figure 1. AWK4573

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PIN CONFIGURATION

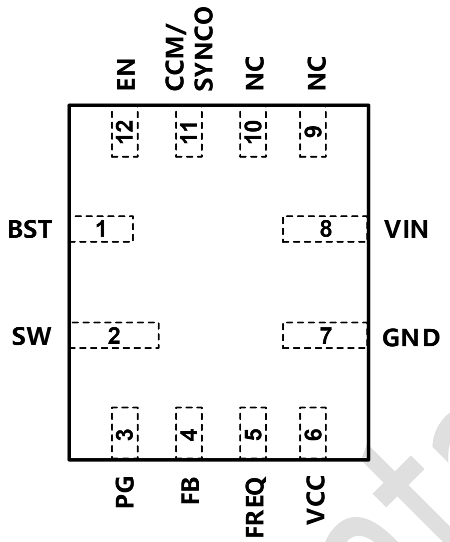

Figure 2. QFN 2.5mmx3mm 12 Pin configuration (Top View)

Table 1. Pin Function Descriptions

Pin No.	Pin Name	Type[1]	Description
1	BST	I/O	Boot-strap. Supply voltage for the internal high-side gate driver. Connect a 0.1µF ceramic capacitor between the SW and BST.
2	SW	P, O	Power Switch Output Pin. Connect to power inductor.
3	PG	O	Open Drain Output Power Good Indicator Pin. Connect a pull up resistor (e.g., 100kΩ) to the system voltage rail.
4	FB	I	Feedback Voltage Sense Input. Connect a resistor divider to set the output voltage.
5	FREQ	I	Switching Frequency Setting Pin. Connect a resistor between FREQ and GND to set the oscillator frequency.
6	VCC	O	Output of the Internal VCC Regulator. Used as supply for the internal control circuits. Do not connect any extra loads. Connect a 1uF ceramic capacitor between this pin and GND pin.

1 Legend:
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin
G=Ground

Pin No.	Pin Name	Type[1]	Description
7	GND	G	Ground.
8	VIN	P, I	Input Power Supply Pin. Connect the power supply to this pin and connect a bypass capacitor between this pin and GND pin.
9, 10	NC	–	No connect. To improve thermal and EMI performance, connect NC pins to Ground.
11	CCM/SYNCO	O	Mode Selection/Synchronous ouput. To force the converter into continuous conduction mode (CCM), connect the CCM/SYNCO pin to GND via a 10kΩ to 300kΩ resistor. Float this pin to force the converter into Pulse Frequency Modulation (PFM) mode under light-load conditions. CCM/SYNCO is also a synchronization output pin that can output a 180° out-of-phase clock to other devices.
12	EN	I	Precision Enable Pin. Drive the EN pin above 1.45V to turn the converter on; float EN or drive it below 1.12V to turn the converter off. An extra resistor divider can be set to create the UVLO.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Min	Max	Unit
V_{IN}	−0.3	63	V
V_{SW}	−0.3	60	V
V_{BST}	−0.3	V_{BST}+6V	V
All other pins	−0.3	6	V
Continuous Power Dissipation		2.08	W
Junction temperature	−40	150	°C
Storage temperature	−65	150	°C
Lead temperature (soldering, 10sec.)		260	°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 3.

Parameters	Min	Typ	Max	Unit
Operating Temperature	−40		125	°C
Continuous Supply Voltage (V_{IN})	3.4		60	V
Output Voltage (V_{OUT})	1% of V_{IN}		98% of V_{IN}	V
Load Current Range	0		3	A
Junction Temperature (T_J)	−40		150	°C

ELECTROSTATIC DISCHARGE (ESD)

Table 4. ESD Rating

Parameters	Description	Rating	Unit
HBM	Human Body Model ANSI/ESDA/JEDEC JS-001-2024 Classification, Class: 2	±2000	V
CDM	Charged Device Mode ANSI/ESDA/JEDEC JS-002-2025 Classification, Class: C2b	±750	V

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance

Item[1,2]	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	60	°C/W
θ_{JC}	Junction-to-case (top) thermal resistance	13	°C/W

(1) The package thermal impedance is calculated in accordance to JESD 51-7.

(2) Thermal Resistances were simulated on a 4-layer, JEDEC board.

ELECTRICAL SPECIFICATIONS

Limits apply over the recommended operating junction temperature range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 24V. VOUT is converter output voltage.

Table 6.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
INPUT SUPPLY AND UNDER-VOLTAGE LOCKOUT (UVLO)						
Quiescent Supply Current	I_Q	No load, V_{FB} =0.8V, PFM		4.6	10	μA
Shutdown Supply Current	I_{SD}	V_{EN}=0V		1.5	5	μA
V_{IN} UVLO Rising Threshold	$V_{IN\_UV\_RISING}$		3.4			V
V_{IN} UVLO Threshold Hysteresis	$V_{IN\_UV\_HYS}$			0.5		V
OUTPUT AND REGULATION						
FB Reference Voltage	V_{REF}		0.784	0.8	0.816	V
FB Input Current	I_{FB}	V_{FB} = 0.85V			20	nA
SWITCHES AND FREQUENCY						
High-Side On Resistance	$R_{DS(ON)\_HS}$	V_{BST}-V_{SW} = 3.5V	100	230	500	mΩ
Low-Side On Resistance	$R_{DS(ON)\_LS}$		20	50	100	mΩ
SW Leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 0V or 60V		0.1	10	μA
Switching frequency	f_{SW}	RFREQ = 76.8kΩ	380	400	420	kHz
		RFREQ = 28kΩ	900	1000	1100	kHz
		RFREQ = 12.1kΩ	2000	2150	2300	kHz
SW Minimum On Time[1]	T_{ON_MIN}			40		ns
SW Minimum Off Time[1]	T_{OFF_MIN}			100		ns
POWER GOOD (PG)						
PG Current Sink	V_{PG_SINK}	Sink 4mA			300	mV
PG Deglitch Time	t_{PG_DELAY}	Rising Edge		80		μs
		Falling Edge		80		μs
PG Leakage Current	I_{PG_LKG}			10	100	nA
PG Rising Threshold (V_{REF})	PG_{RISING}	VFB Rising	87	90	93	%
		VFB Falling	104	109	114	%
PG Falling Threshold (V_{REF})	$PG_{FALLING}$	VFB Falling	82	85	89	%

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[1] Derived from bench characterization. Not tested in production.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
		VFB Rising	112	116	121	%
ENABLE (EN)						
EN Rising Threshold	V_{EN_RISING}		1.38	1.45	1.52	V
EN Falling Threshold	$V_{EN\_FALLING}$		1.09	1.12	1.16	V
EN Threshold Hysteresis	V_{EN_HYS}			330		mV
EN Input Current	I_{EN}	V_{EN} = 2V		0.7		µA
EN Turn-off Delay	t_{EN_DELAY}		5			µs
BOOTSTRAP(BST)						
(BST-SW) UVLO				2.25	2.5	V
SOFT START (SS) AND VCC						
Soft-Start Time	t_{SS}			0.7		ms
VCC Regulator	V_{CC}	I_{CC} = 0mA	3.4	3.55	3.7	V
PROTECTIONS						
Peak Current Limit Threshold	I_{PEAK_LIMIT}	20% duty cycle	4.1	5.1	5.7	A
Valley Current Limit Threshold	I_{VALLEY_LIMIT}		3			A
Zero-Current Detection (ZCD) Threshold	I_{ZCD}	PFM		0.15		A
Negative current limit threshold	I_{NEG_LIMIT}	FCCM		1		A
Thermal Shutdown	T_{SD}			170		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}			25		℃

TYPICAL CHARACTERISTICS

V_{IN} = 24V, T_J = –40°C to +125°C, unless otherwise noted.

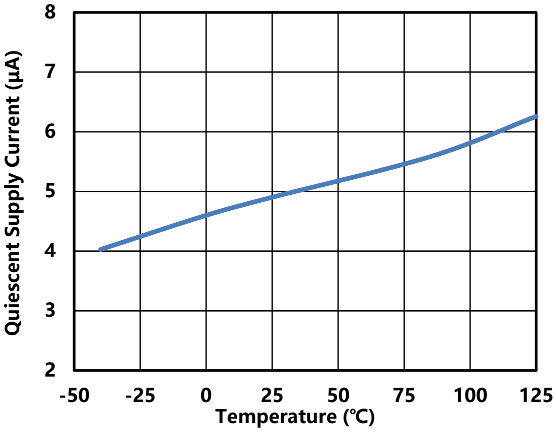


Figure 3. Quiescent Supply Current vs. Temperature

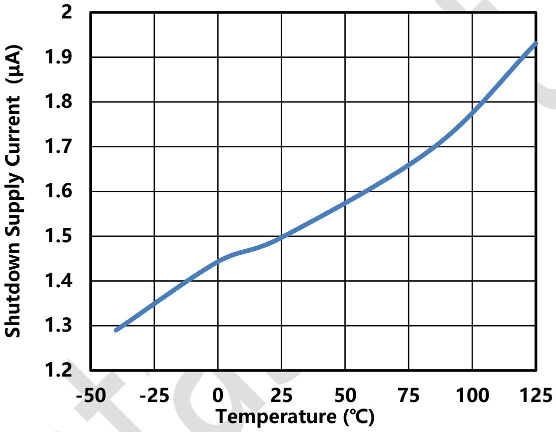


Figure 4. Shutdown Current vs. Temperature

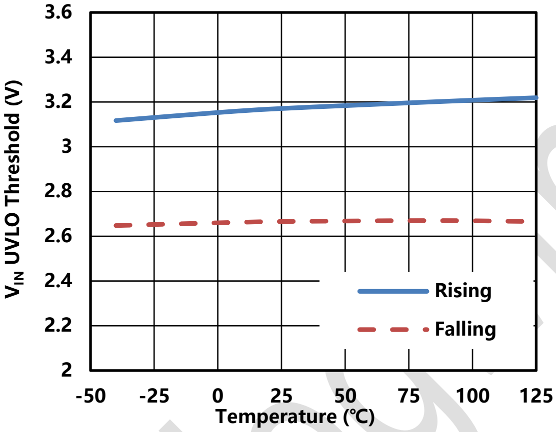


Figure 5. V_{IN} UVLO Threshold vs. Temperature

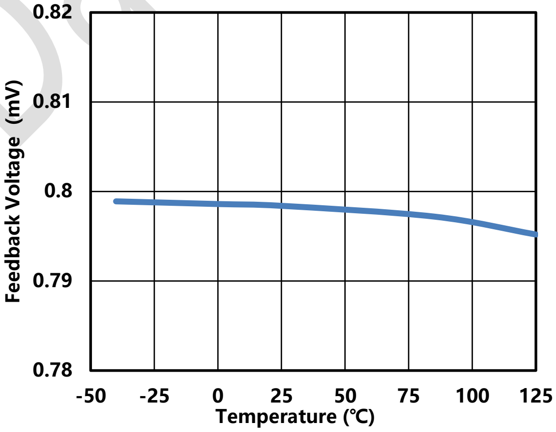


Figure 6. Feedback Voltage vs. Temperature

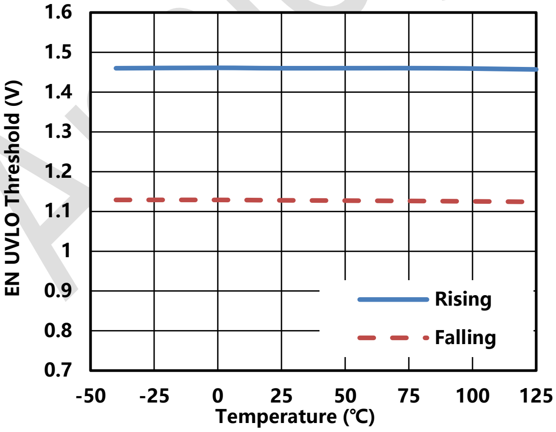


Figure 7. EN Threshold vs. Temperature

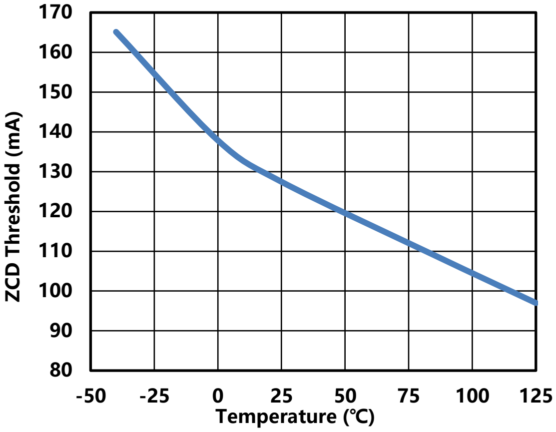


Figure 8. ZCD Threshold vs. Temperature

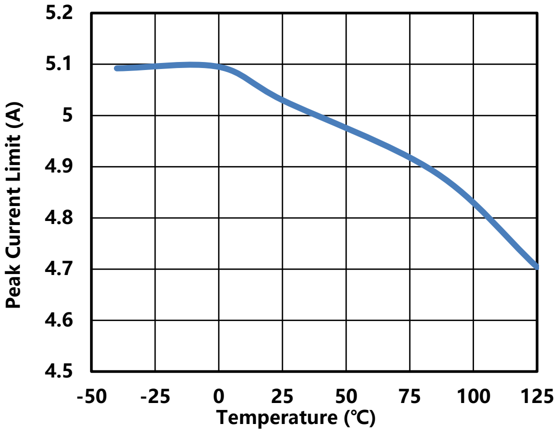


Figure 9. Peak Current Limit vs. Temperature

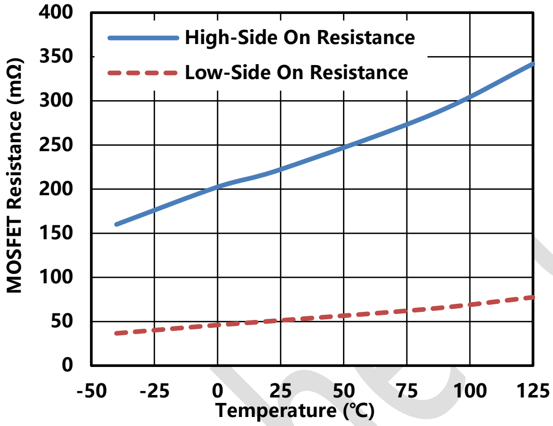


Figure 10. MOSFET Resistance vs. Temperature

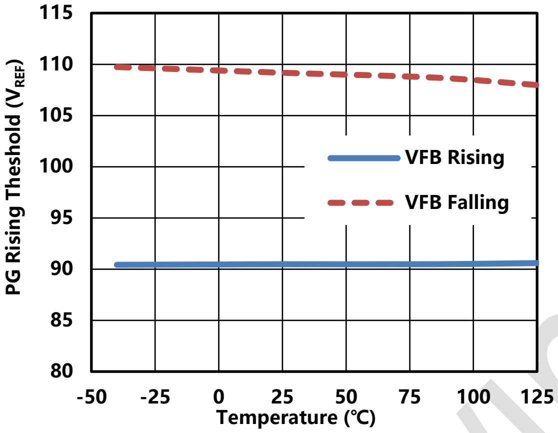


Figure 11. PG Rising Threshold vs. Temperature

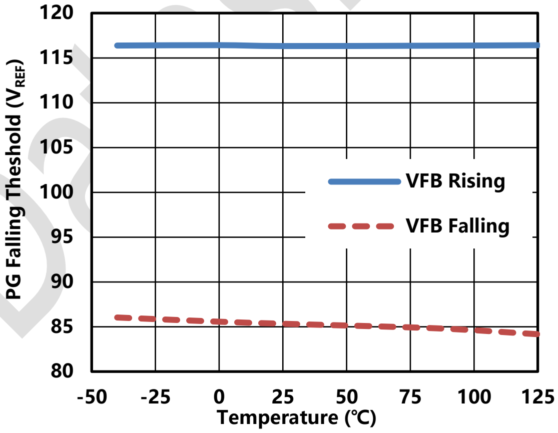


Figure 12. PG Falling Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 5V, L = 15µH(1), f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

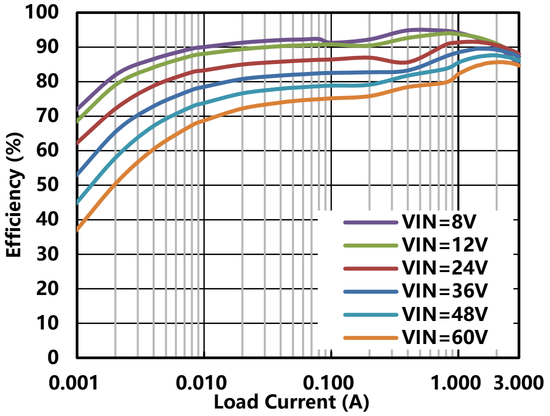


Figure 13. Efficiency vs. Load Current (PFM, f_{SW} = 400kHz, L=15µH)

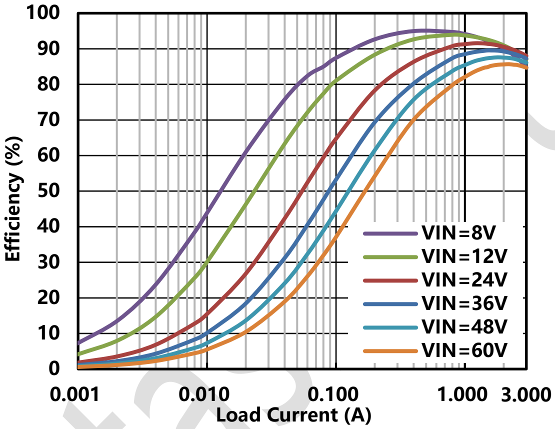


Figure 14. Efficiency vs. Load Current (FCCM, f_{SW} = 400kHz, L=15µH)

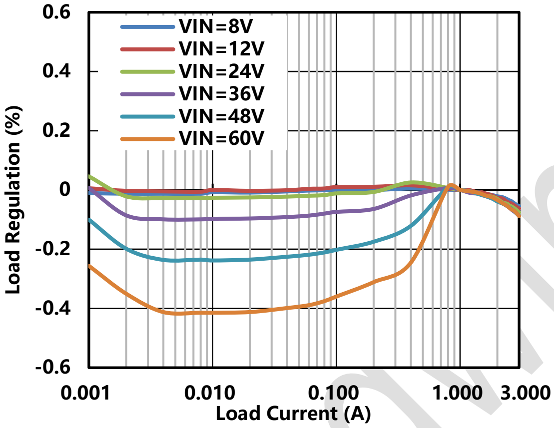


Figure 15. Load Regulation (PFM, f_{SW} = 400kHz, L=15µH)

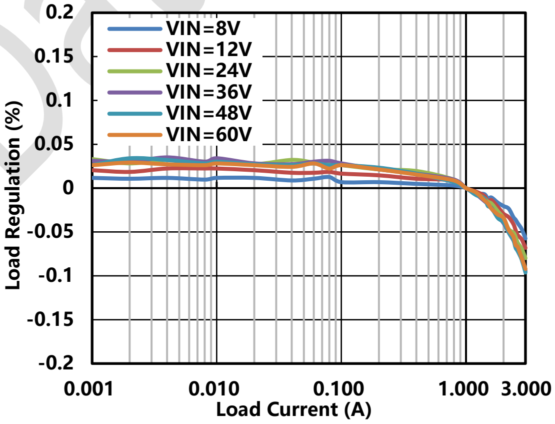


Figure 16. Load Regulation (FCCM, f_{SW} = 400kHz, L=15µH)

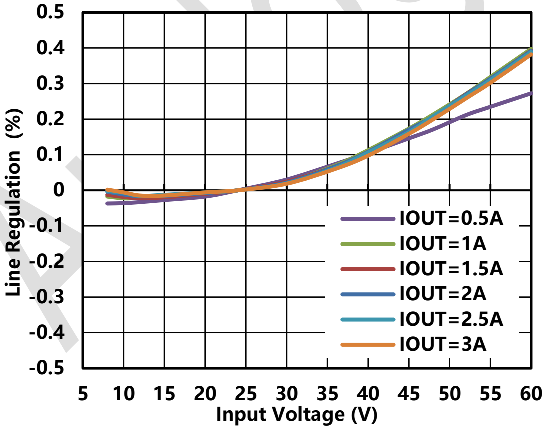


Figure 17. Line Regulation (PFM)

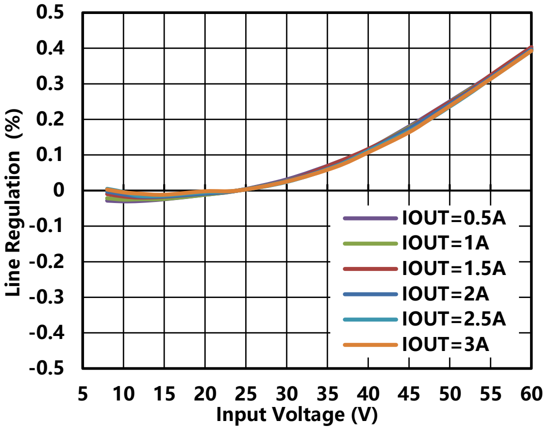


Figure 18. Line Regulation (FCCM)

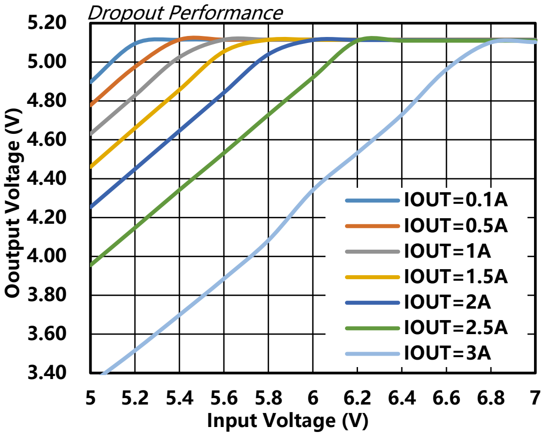


Figure 19. Output Voltage vs. Input Voltage (PFM, f_{SW} = 400kHz, L=15μH)

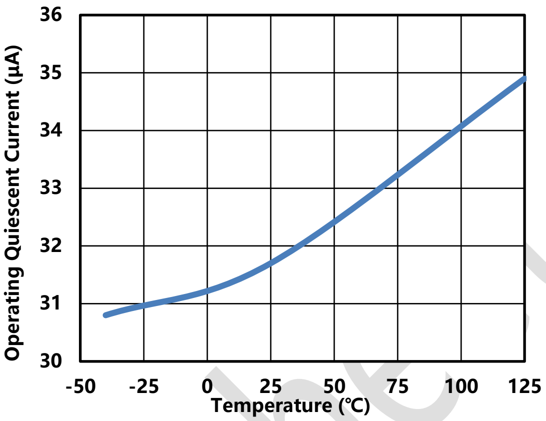


Figure 20. Operating Quiescent Current vs. Temperature

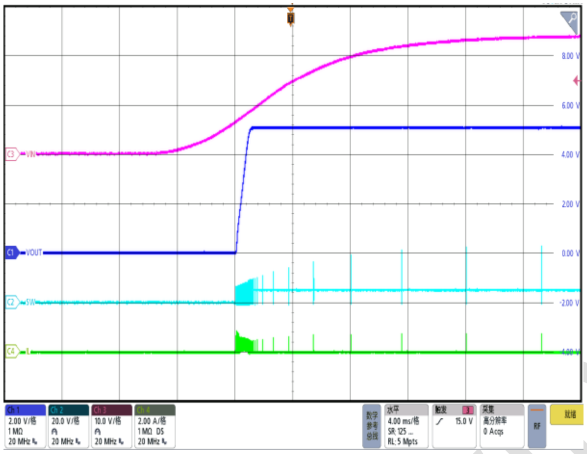


Figure 21. Power On by VIN, I_{OUT}=0A, PFM

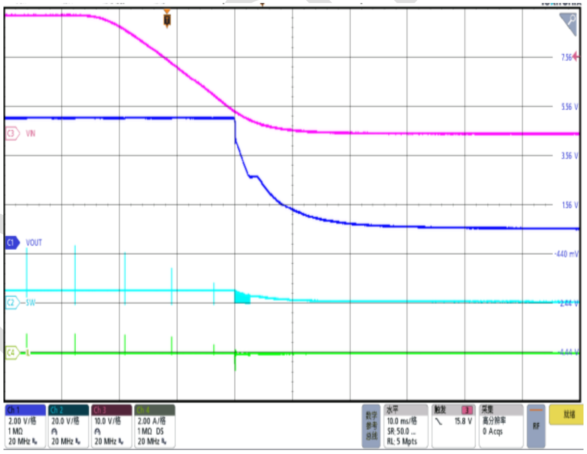


Figure 22. Power Off by VIN, I_{OUT}=0A, PFM

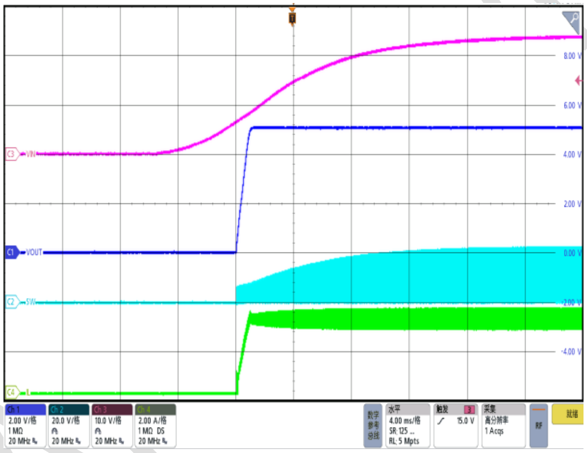


Figure 23. Power On by VIN, I_{OUT}=3A, PFM

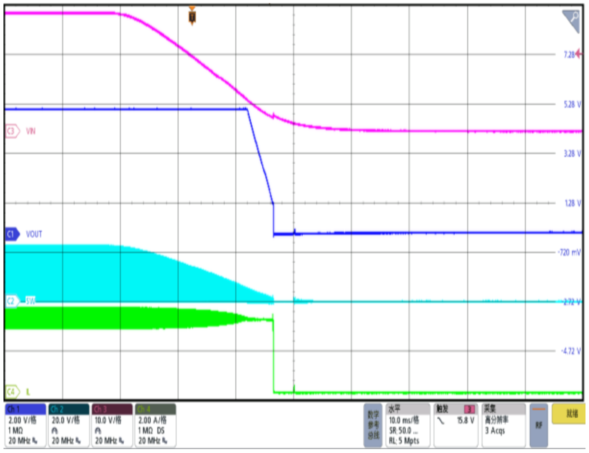


Figure 24. Power Off by VIN, I_{OUT}=3A, PFM

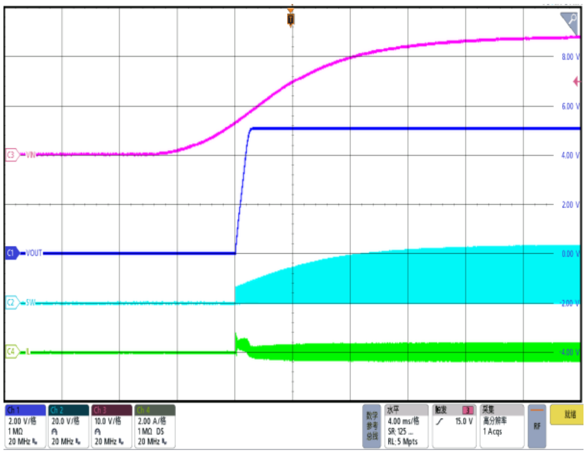


Figure 25. Power On by VIN, I_{OUT}=0A, FCCM

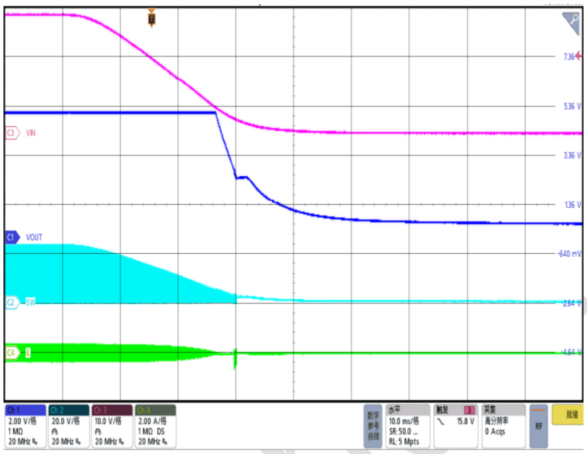


Figure 26. Power Off by VIN, I_{OUT}=0A, FCCM

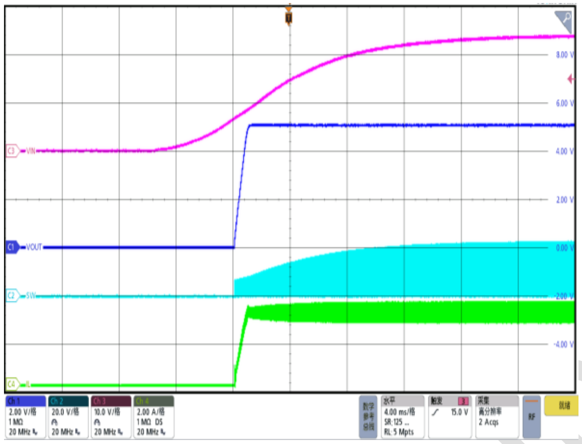


Figure 27. Power On by VIN, I_{OUT}=3A, FCCM

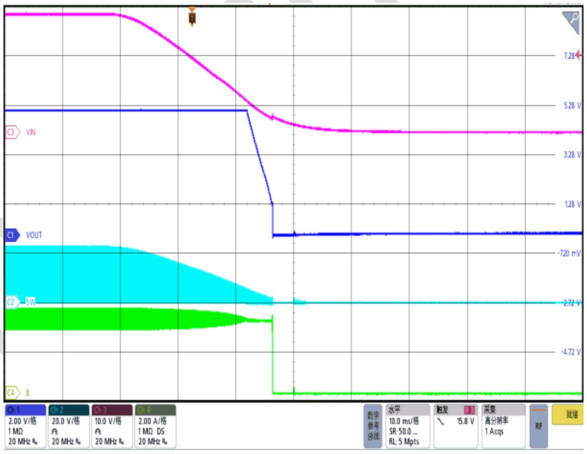


Figure 28. Power Off by VIN, I_{OUT}=3A, FCCM

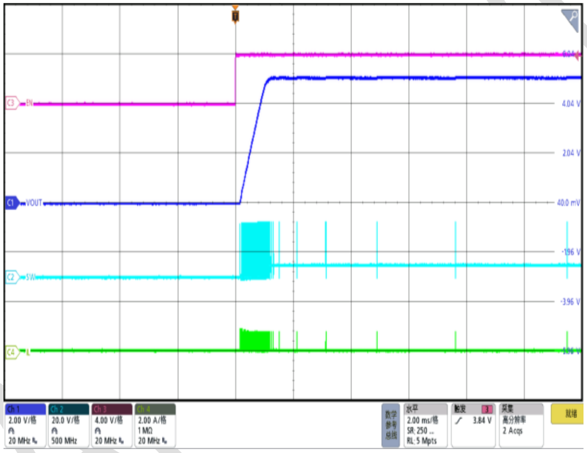


Figure 29. Power On by EN, I_{OUT}=0A, PFM

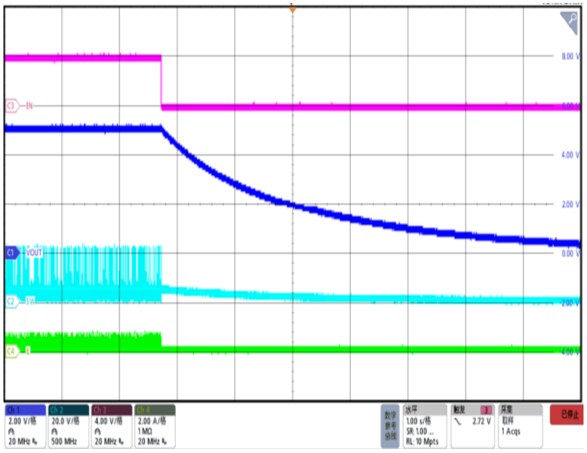


Figure 30. Power Off by EN, I_{OUT}=0A, PFM

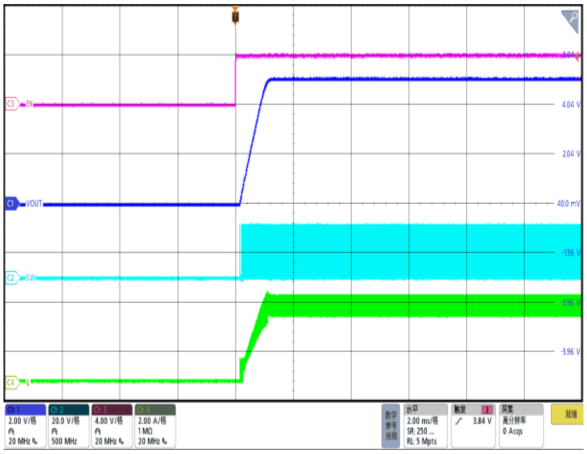


Figure 31. Power On by EN, I_{OUT}=3A, PFM

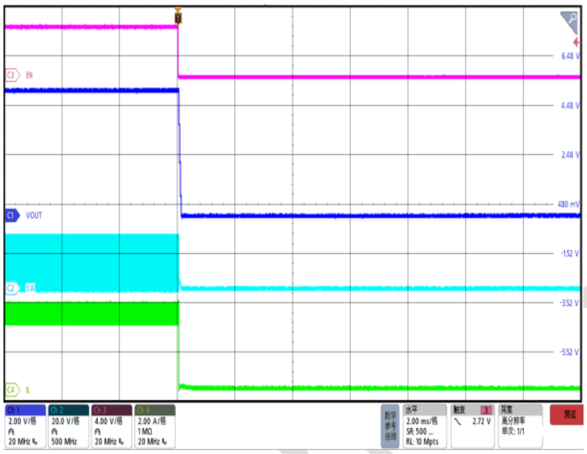


Figure 32. Power Off by EN, I_{OUT}=3A, PFM

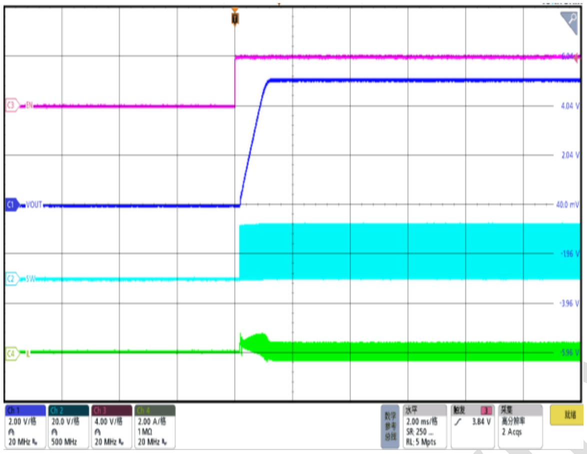


Figure 33. Power On by EN, I_{OUT}=0A, FCCM

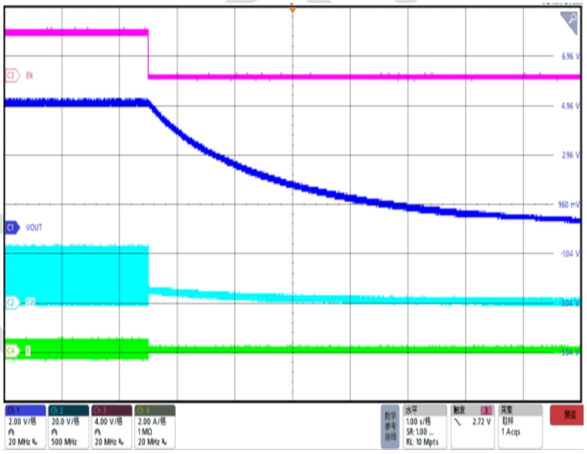


Figure 34. Power Off by EN, I_{OUT}=0A, FCCM

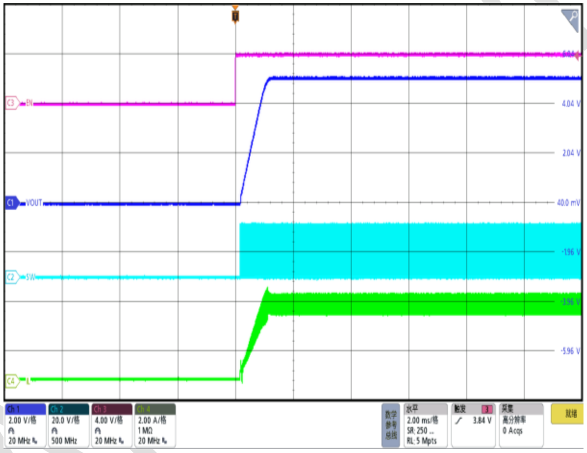


Figure 35. Power On by EN, I_{OUT}=3A, FCCM

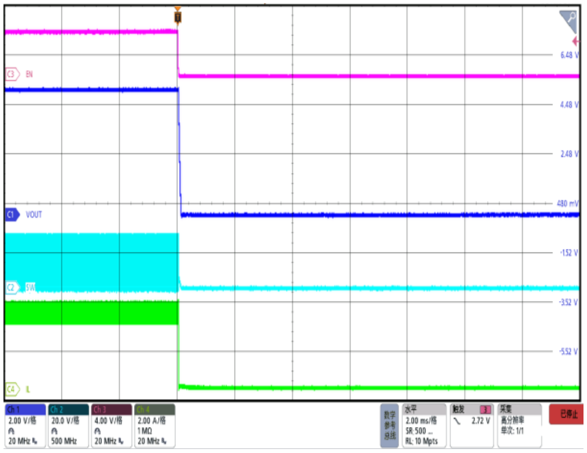


Figure 36. Power Off by EN, I_{OUT}=3A, FCCM

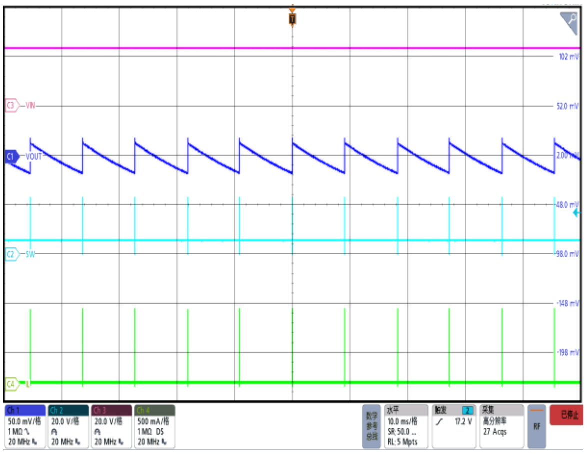


Figure 37. Switching Waveform, I_{OUT}=0A, PFM

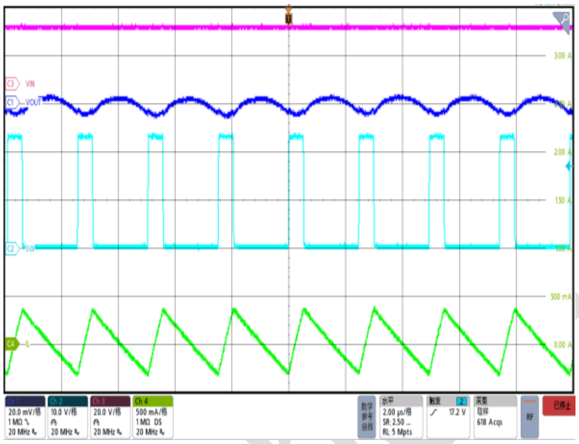


Figure 38. Switching Waveform, I_{OUT}=0A, FCCM

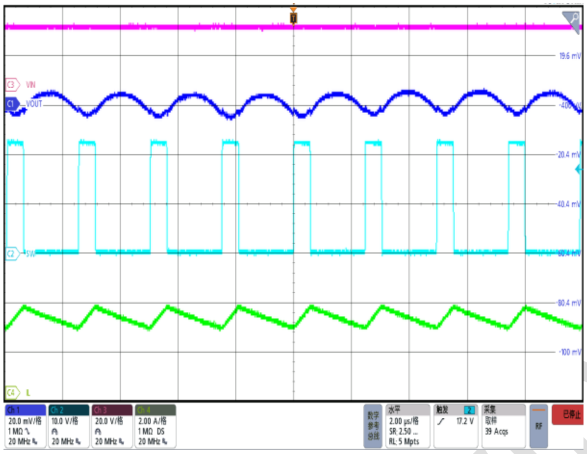


Figure 39. Switching Waveform, I_{OUT}=3A, PFM

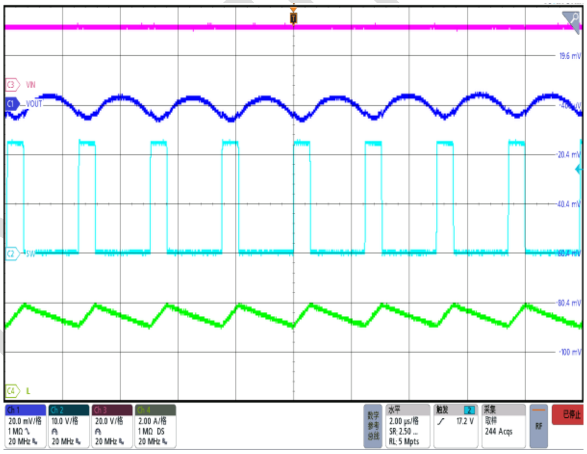


Figure 40. Switching Waveform, I_{OUT}=3A, FCCM

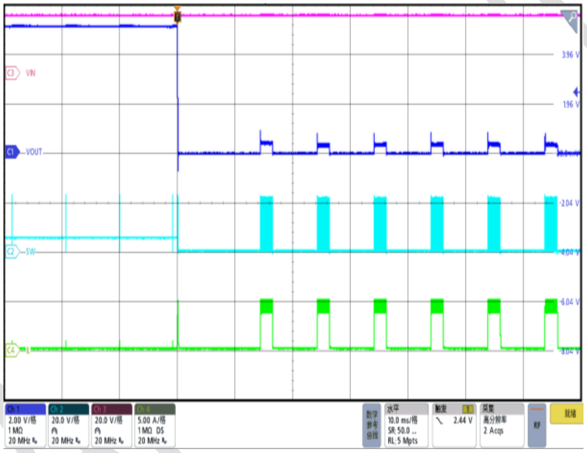


Figure 41. SCP Entry, I_{OUT}=0A, PFM

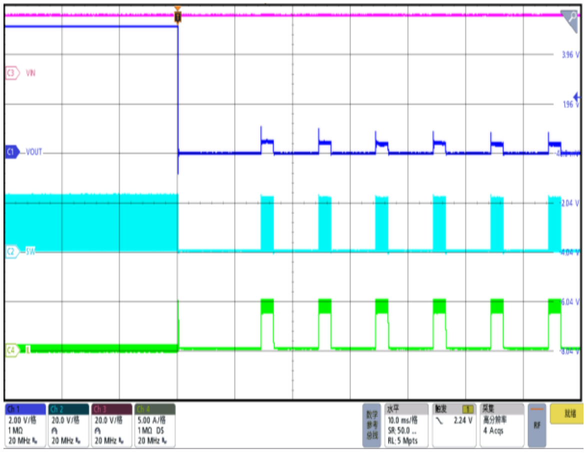


Figure 42. SCP Entry, I_{OUT}=0A, FCCM

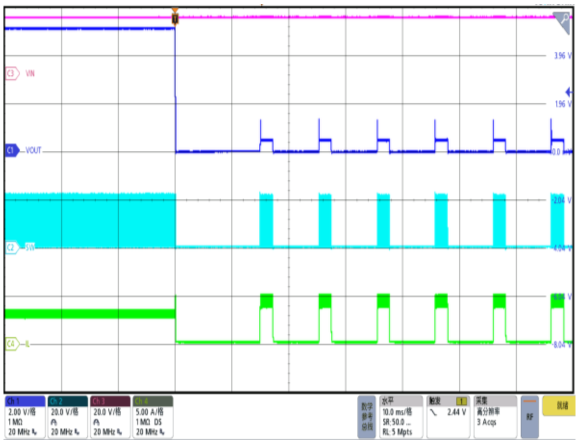


Figure 43. SCP Entry, I_{OUT}=3A, PFM

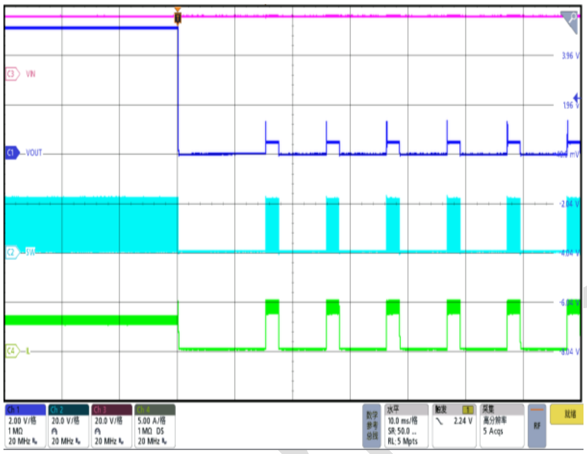


Figure 44. SCP Entry, I_{OUT}=3A, FCCM

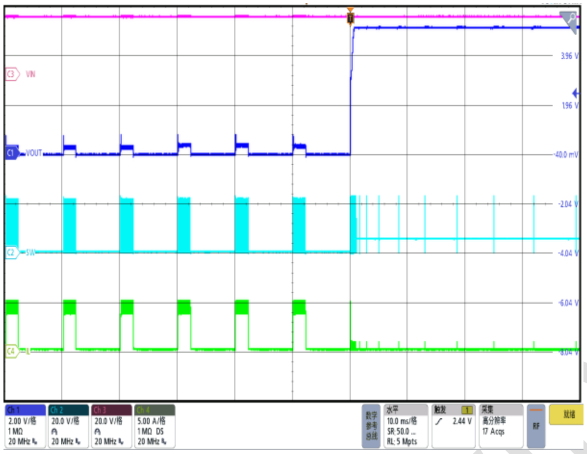


Figure 45. SCP Recovery, I_{OUT}=0A, PFM

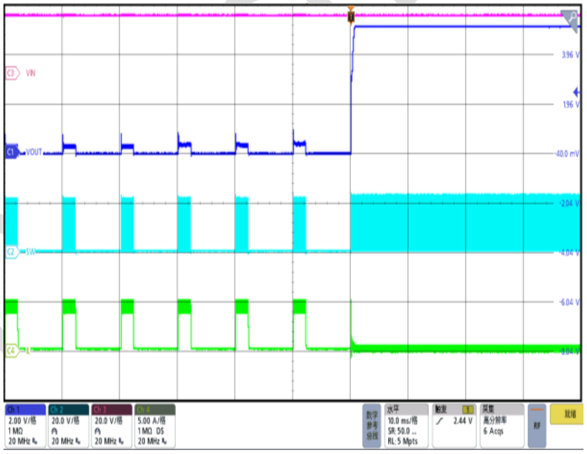


Figure 46. SCP Recovery, I_{OUT}=0A, FCCM

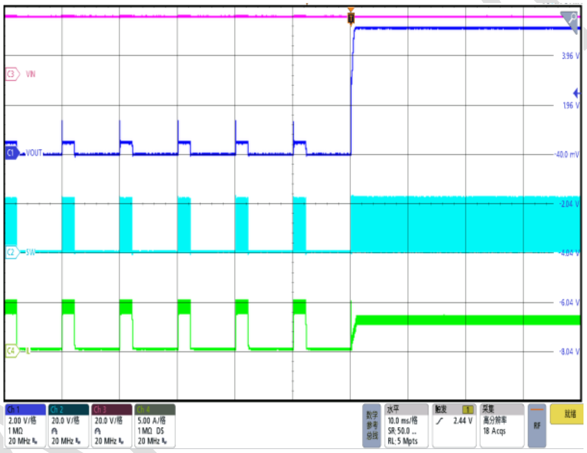


Figure 47. SCP Recovery, I_{OUT}=3A, PFM

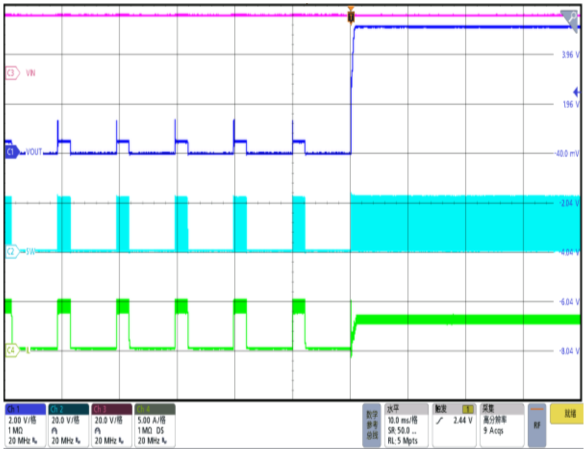


Figure 48. SCP Recovery, I_{OUT}=3A, FCCM

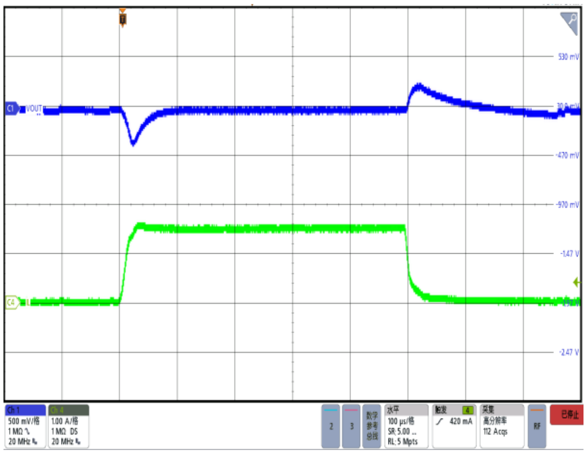


Figure 49. Load Transient, I_{OUT}=0A to 1.5A, PFM

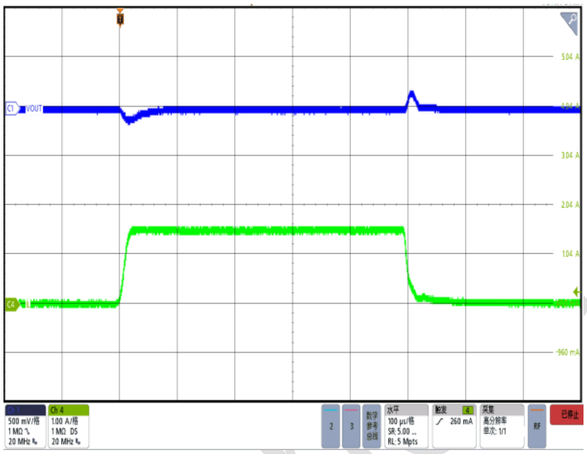


Figure 50. Load Transient, I_{OUT}=0A to 1.5A, FCCM

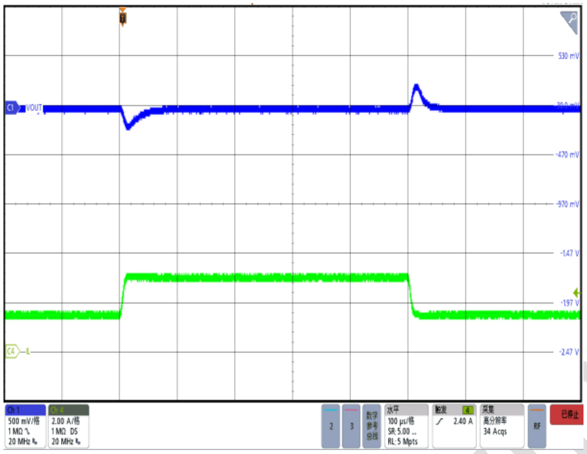


Figure 51. Load Transient, I_{OUT}=1.5A to 3A, PFM

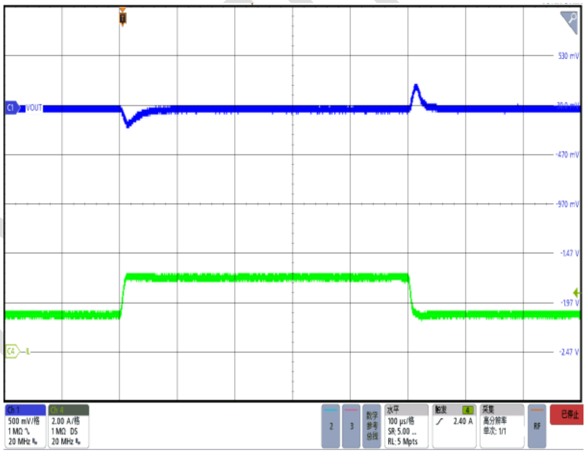


Figure 52. Load Transient, I_{OUT}=1.5A to 3A, FCCM

Note:

(1) Inductor PN: XAL6060-153MEB/C; DCR=43.75mΩ.

FUNCTIONAL BLOCK DIAGRAM

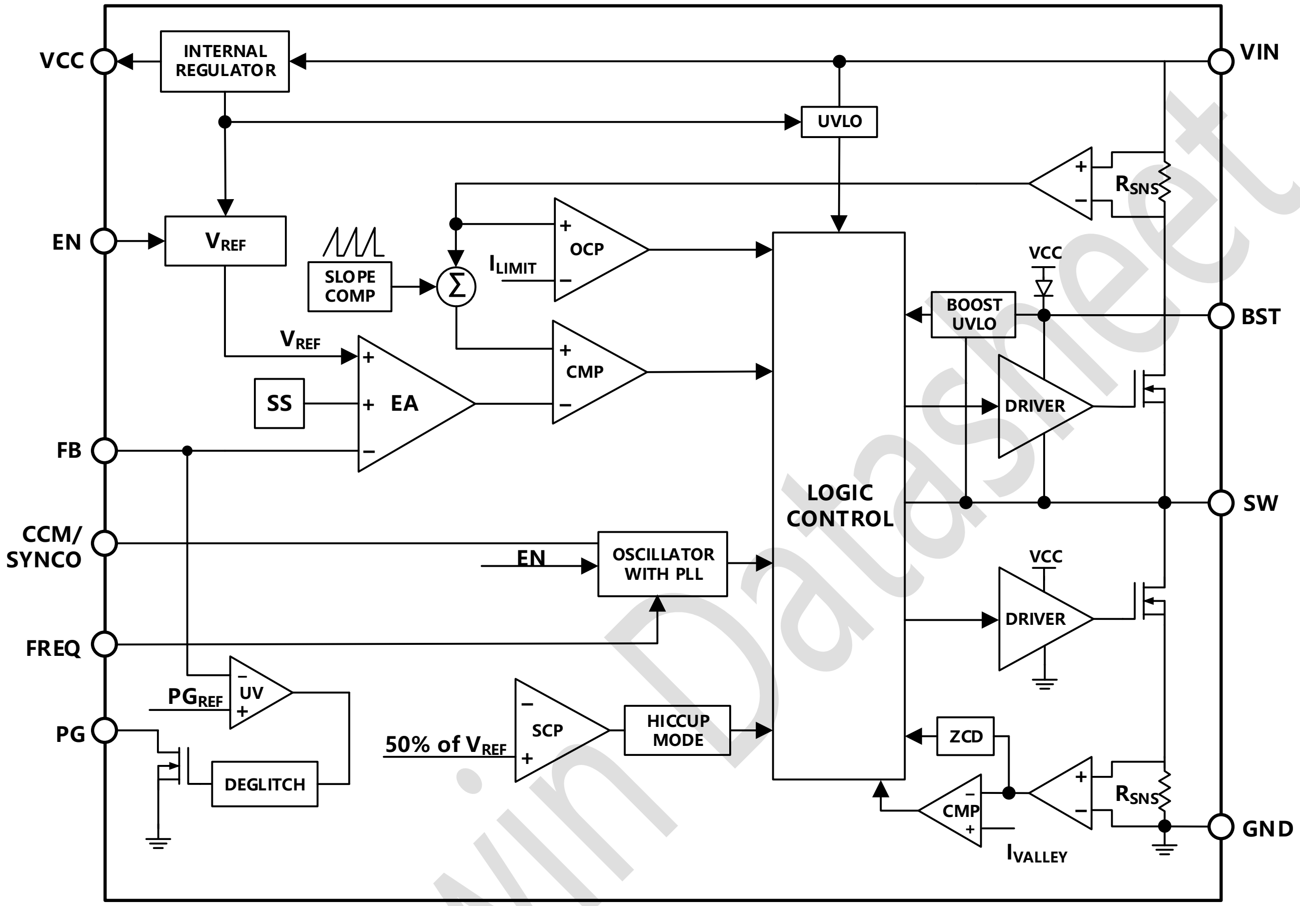


Figure 53. Functional Block Diagram

PRODUCT OVERVIEW

The AWK4573 is a synchronous step-down, DC-DC regulator with a high-side MOSFET and a low-side synchronous rectifier MOSFET. The AWK4573 operates a wide range of 3.4V to 60V input voltage and the device is capable of delivering up to 3A continuous current load. This converter is highly adaptable to Industrial and telecom environment applications which require high performance.

It employs peak-current-mode control to regulate the output voltage. In the light load conditions, the device provides selectable Pulse Frequency Modulation (PFM) for higher efficiency or Forced Continuous Conduction Mode (FCCM) for smaller output ripple. In the heavy load conditions, the device runs in the Pulse Width Modulation (PWM) mode at a constant frequency. The switching frequency is configured by the FREQ resistor. The regulator is internally compensated, which allows few external components and reduces design time.

The AWK4573's protection features include undervoltage lockout, over current protection, short-circuit protection, thermal shutdown. Additional features include the following: low shutdown current; internal soft start; precision enable; Power good indication; synchronous output function; pre-biased start up.

PEAK CURRENT CONTROL

The AWK4573 uses fixed frequency peak current mode control architecture. The inductor current increases when the integrated high-side MOSFET turns on, and the high side MOSFET turns off when the inductor peak current reaches the peak threshold set by the comp voltage of the internal error amplifier, while the low side synchronous rectifier MOSFET turns on until the next cycle or the inductor current falls to zero.

The error amplifier of the AWK4573 servos the comp voltage by comparing the voltage of the FB pin with the internal 0.8V reference. When the load current increases, it causes a reduction in FB voltage relative to the internal reference. This issue causes the error amplifier raise the comp voltage, to increase the inductor peak current till the enough power maintains the output voltage in regulation. Meanwhile, the AWK4573 integrated a slope compensation circuitry to avoid the subharmonic oscillation phenomenon when the duty cycle is above 50%.

LIGHT-LOAD OPERATION

The AWK4573 features configurable forced continuous conduction mode (FCCM) and Pulse Frequency Modulation (PFM) mode. FCCM maintains a constant switching frequency (f_{SW}) and small output ripple, but has low efficiency under light-load conditions. PFM mode is set by the CCM/SYNCO pin and achieves high efficiency under light-load condition. To force the device into FCCM, use a 10kΩ to 300kΩ resistor to connect CCM/SYNCO to GND.

In FCCM mode, the converter operates at a fixed frequency across a no-load to full-load range. Under light-load conditions, float CCM/SYNCO to force the device into PFM mode. The device cannot change modes once it is turned on; the desired mode must be selected before start-up.

In PFM Mode, f_{SW} scales down according to COMP voltage. When I_{OUT} decreases, an increment in the feedback voltage causes COMP voltage to drop. When COMP voltage falls to a low clamp threshold, the device enters PFM mode. In PFM mode, the output voltage decreases due to output capacitor discharging. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold, enabling the high-side power MOSFET turns on at next clock pulse. After this clock, COMP voltage drops again and is clamped and PFM mode repeats. This control scheme improves efficiency by scaling down the frequency to reduce switching and gate driver losses while minimizing the input quiescent current.

As I_{OUT} increases from light-load, both COMP voltage and f_{SW} rise. If I_{OUT} exceeds a critical level (the continuous current boundary), the inductor current becomes continuous, and the converter transitions from Discontinuous Conduction Mode (DCM) into Continuous Conduction Mode (CCM). In CCM, the switching frequency remains constant.

PRECISION ENABLE AND SHUTDOWN

The AWK4573 uses EN pin to implement start-up and shutdown condition. This input pin features precision analog threshold of 1.45V. When a voltage on the EN pin is greater than 1.45V, the converter turns on; when the voltage falls to less than 1.12V, the converter is required to shut down. When driving the EN pin from VIN (or any voltage above its absolute maximum rating), a protection network is required. Connect a 100kΩ resistor from VIN to EN, and clamp the EN pin to ground with a 5.6V Zener diode. To shut down the converter, float EN via an internal resistor from EN to GND. If enable (EN) control is on, then R_{EN} = 2.8MΩ. If EN control is off, then R_{EN} = 1.8MΩ.

INTERNAL VCC REGULATOR

The VCC pin is the output of the internal regulator, which provides the bias for the internal circuits and MOSFET GATE drivers. It is recommended that a high quality 1uF ceramic capacitor should be connected from this pin to GND. It is not recommended to connect to any external loads on VCC pin.

BOOTSTRAP CIRCUITRY

The bootstrap voltage provides the gate drive power for high-side MOSFET. The capacitor voltage is charged via a diode from V_{CC} when high-side MOFET is off and low-side MOSFET is on, which generates a bootstrap voltage between the BST and SW pins. It is recommended that a 0.1uF, 10V ceramic capacitor should be connected from BST pin to SW pin.

SYNCHRONOUS OUTPUT (SYNCO)

The AWK4573 has a SYNCO pin for synchronous output. During start-up, SYNCO remains low and outputs a 180° phase-shift clock to the internal oscillator once soft start (SS) is ready. SYNCO's falling edge is a 180° phase shift from the rising edge of the internal oscillator. The synchronous output function allows two devices to operate at the same frequency, but 180° out of phase. This reduces the total input current ripple and allows for the use of a smaller input bypass capacitor.

SWITCHING FREQUENCY

The AWK4573's switching frequency is controlled by the single FREQ resistor on FREQ pin. The resistor value can be calculated from the following equation:

$$R_{FREQ}(k\Omega) = \frac{30000}{f_{sw}(kHz)}$$

For example, a 76.8kΩ resistor sets the switching frequency to 400kHz, a 28kΩ resistor sets the frequency to 1MHz, and a 12.1 kΩ resistor sets the switching frequency to 2.2MHz. A bench test may be required to fine-tune the calculated resistance. Table 7 shows the typical relationship between f_{sw} and R_{FREQ}.

Table 7. SWITCHING FREQUENCY vs. R_{FREQ}

R_{FREQ}(kΩ)	f_{sw}(kHz)	R_{FREQ}(kΩ)	f_{sw}(kHz)
100	300	24.3	1150
91.9	330	22	1250
82.5	360	20	1350
76.8	400	18.2	1500
68.1	430	16.2	1650
61.9	475	15	1750
56	520	14	1900
47	600	13	2050
39	700	12.1	2200
34.8	800	11.5	2250
30	940	11	2350
28	1000	10	2500

SPREAD SPECTRUM MODULATION

The AWK4573 implements the Spread Spectrum Modulation (SSM) to reduce EMI for most automotive application. The SSM circuitry modulates the switching frequency of the converter periodically within a certain frequency range around the configured switching frequency by using a triangular frequency modulation and the periodical jittering span is approximately 18% (typ. for f_{SW} = 400kHz) higher than the programmed frequency. (The modulation frequency is approximately 3kHz.) The modulation is fixed by factory only for AWK4573AA.

INTERNAL SOFT START (SS) AND PREBIAS SOFT START

The AWK4573 features integrated reference-based soft start circuitry to limit output voltage rising time and prevent output voltage overshoots and inrush current at start up. During SS, V_{OUT} ramps up at a controlled slew rate once EN goes high.

The device tracks the lowest voltage including the internal reference voltage, the internal soft-start voltage and the SS pin voltage as the reference, which the amplifier regulates the FB voltage to. If the soft-start voltage (V_{SS}) drops below the internal reference voltage (V_{REF}), V_{SS} overrides V_{REF} as the EA reference. The soft start completes when the V_{SS} exceeds the V_{REF} of 0.8V. Once SS is complete, the AWK4573 enters steady state operation.

The soft start time is fixed internal 0.7ms. If V_{OUT} shorts to GND, V_{FB} is pulled low and V_{SS} discharges. Once the short is removed and the AWK4573 returns to a normal state, the device initiates another SS.

If the output voltage is pre-biased in an initial voltage before the AWK4573 start up, neither the high-side MOSFET or the low-side MOSFET of the device turns on to initiates switching until the internal reference voltage has reached the V_{FB}. The output is not pulled low during the pre-biased start up condition. This capability is only available when the device is in PFM mode.

POWER GOOD FUNCTION

The Power good pin is an open-drain output, which indicates that the FB pin voltage is within regulation and indicates to simplify the sequencing. It is recommended that the PG pin should be tied through an external pullup resistor, about 100kΩ to a suitable logic supply if this function is needed; if not, the PG pin must be left floating.

The PG internal circuitry monitors the FB pin voltage and compares it to the rising and falling thresholds, which operation can be understood by Figure 54.

The PG pin continues to be forced low if multiple events occurred, including the output voltage decreasing below the FB falling threshold or exceeding the rising voltage, UVLO, OVP, current limit, thermal shutdown, disable state.

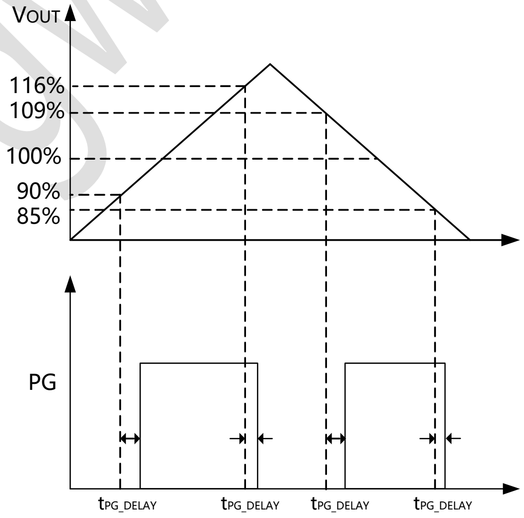


Figure 54. PG-timing behavior

UNDERVOLTAGE LOCKOUT (UVLO)

The AWK4573 features the undervoltage lockout protection for the occurrence of power-on glitch. With the EN pin is enable, once the V_{IN} pin voltage exceeds the UVLO rising threshold, the internal circuitry is activated and soft start period is initiated. If the V_{IN} drops below the falling threshold, the device shuts down. V_{IN} UVLO is a non-latch protection.

OVER CURRENT PROTECTION AND SHORT CIRCUIT PROTECTION

The AWK4573 implements over current protection with cycle-by-cycle limiting inductor peak current and valley current to prevent current running away during the heavy loads or output hard short condition. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for hard short circuits. The internal sensing circuitry monitors the high-side MOSFET current while it turns on.

If the high-side MOSFET current exceeds the 5.1A peak current-limit threshold, it turns off immediately. The low-side MOSFET turns on, and the current goes through it, which is also monitored. The low-side MOSFET is kept on until the inductor current ramps below the 3A valley current limit threshold.

If the short circuit condition occurs, the AWK4573 reaches its peak current limit and V_{OUT} drops until V_{FB} is below 50% of V_{REF} after soft start. The device triggers Short-Circuit Protection, and enters hiccup mode. In hiccup mode, the high-side and low-side MOSFETS are both turn off before the AWK4573 attempts to restart. If the over current or short circuit fault is removed, the AWK4573 recovers to normal operation. Otherwise, hiccup repeats, which can protect the device from over-heating, over dissipation under heavy loads condition and potential damage.

NEGATIVE CURRENT LIMIT PROTECTION

The AWK4573 features a 1A negative current limit threshold. If I_L drops below the negative current

limit, the low-side MOSFET turns off and the high-side MOSFET turns on. This prevents the negative current from dropping too low and potentially damaging the components.

THERMAL SHUTDOWN

The AWK4573 monitors the die temperature. If the junction temperature exceeds 170℃, the internal thermal shutdown circuitry turns off the regulator, stops the MOSFET switching, pulls down the SS. Thermal shutdown is a non-latch protection, when the junction temperature falls below to 145℃, the part resumes normal operation with soft start automatically.

LOW-DROPOUT (LDO) MODE

If the condition of low voltage difference from the V_{IN} and V_{OUT} occurs, the AWK4573 operates at as close to 100% duty cycle as possible in Low-Dropout (LDO) mode, as long as the voltage between BST and SW exceeds 2.25V. When the voltage from BST to SW drops below 2.25V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor. If V_{IN} drops, the high-side MOSFET continues to operate as approaching to 100% duty as possible to maintain output regulation, unless the voltage between BST and SW falls below 2.25V.

During slowing power up and power down application, the off-time of the high-side MOSFET starts to approach the minimum value, so that the output voltage can closely track the input voltage ramping down.

The effective duty cycle during regulator dropout is primarily influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and PCB resistance.

TYPICAL APPLICATION CIRCUIT

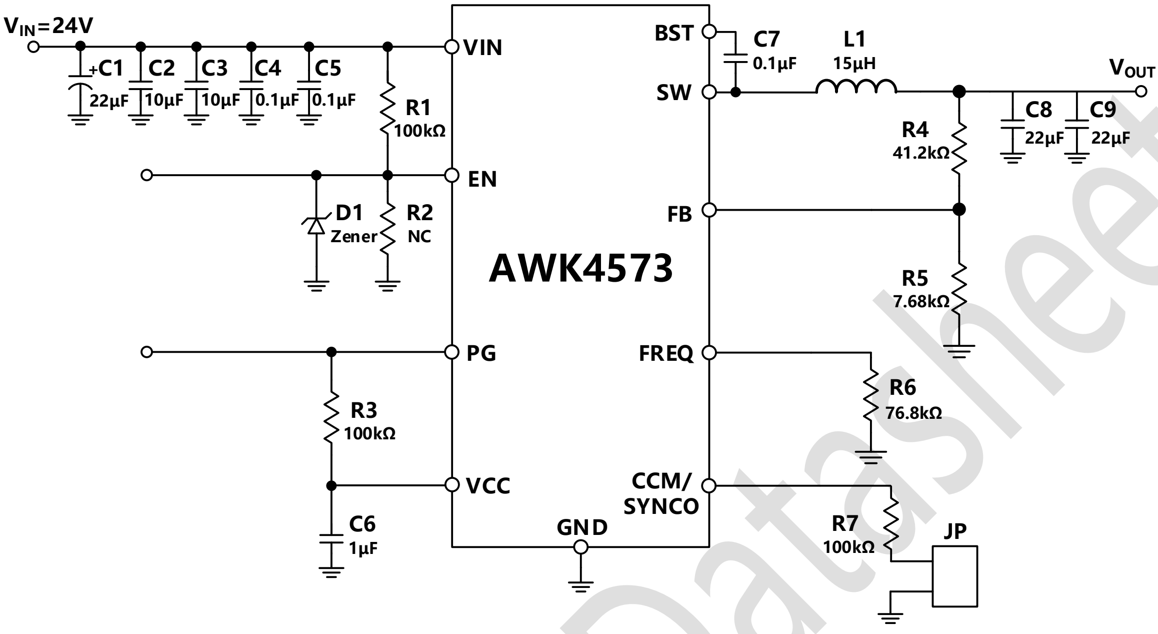


Figure 55. Typical Application Circuit (400kHz)

APPLICATION INFORMATION

Component selection steps are described in this section based on the example specifications listed in Table 8. The schematic of this design example is showed in Figure 55. Typical Application Circuit (400kHz)

Table 8. Parameter of Design Example

Parameter	Description
Input Voltage	V_{IN}=24V
Output Voltage	V_{OUT}=5V
Output Current	I_{OUT}=3A
Switching Frequency	f_{SW}=400kHz
Output Ripple	ΔV_{OUT_RIPPLE}=15mV
Load Transient	±5%，1.5A to 3A

INPUT CAPACITOR SELECTION

The step-down converter has a discontinuous input current, therefore it requires a capacitor to supply the AC to the converter while maintaining the DC V_{IN}. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended because of the low ESR and small temperature coefficients. To filter the high frequency switching noise, it is recommended that use a lower value capacitor(0.1uF) with 0603 package size. Place the input capacitor as close as possible to the Vin pin. For most applications, a 22µF capacitor is sufficient. For higher VOUT, use a 47µF capacitor to improve system stability.

The voltage rating of the input capacitor must be greater than the maximum input voltage. The input capacitor value is a function of the source impedance, one bulk capacitor is needed if the source impedance is over high. Make sure that the ripple current rating should not exceed the converter's maximum input ripple current calculated from the following equation:

$$I_{C_{IN}\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, where

$$I_{C_{IN}\_RMS} = \frac{I_{OUT}}{2}$$

For simplification, choose a CIN with an RMS current rating greater than half of the maximum load current.

Ensure that the voltage rating of the input capacitor must be greater than the maximum input voltage. The input voltage ripple caused by the capacitance can be calculated from the following equation:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{OUT}} \times D \times (1-D)$$

OUTPUT VOLTAGE SETTING

The output voltage of the AWK4573 is set by the external resistor divider. Use the following equation to calculate resistor values:

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{TOP}}{R_{BOT}})$$

Where:

V_{REF} is the typical reference value, 0.8V.

Table 9 lists the recommended resistor divider values of R_{TOP}, R_{BOT} for the common output voltages .

Table 9. Recommended Resistor Values for Common Output Voltages

V_{OUT}(V)	R_{TOP}(kΩ)	R_{BOT}(kΩ)
3.3	41.2	13
5.0	41.2	7.68
8	41.2	4.53
12	41.2	2.98

INDUCTOR SELECTION

The inductor value is determined by the switching frequency, input voltage, output voltage, and inductor ripple current. For the highest efficiency, choose an inductor with a low DC resistance. The performance of the inductor affects the transient behavior, efficiency, loop stability. Using a larger inductor value reduces the output ripple current and then reduces the output voltage ripple, and also leads to better efficiency, but it leads to slower transient behavior. A smaller inductor value offers a fast transient behavior, but it leads to larger inductor ripple current and then decreases efficiency.

The inductor value can be calculated by the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:

V_{IN} is the input voltage.

V_{OUT} is the output voltage.

D is the duty cycle ($D = \frac{V_{OUT}}{V_{IN}}$)

f_{SW} is the switching frequency.

ΔI_L is the inductor ripple current, which is, for the most applications, typically between 20% and 40% of the maximum load current.

The peak inductor current, I_{PEAK} is calculated by the following equation:

$$I_{PEAK} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor must be higher than the device's peak current limit, and RMS current must also not be exceeded, as the following equation:

$$I_{RMS} = \sqrt{(I_{OUT})^2 + \frac{\Delta I_L^2}{12}}$$

OUTPUT CAPACITOR SELECTION

The output capacitor determines the output ripple and it stores energy to satisfy the transient loads and the loop stability of the regulator. The selection of the output capacitor is based on two parts. One is determined by the inductor ripple current going through the ESR of the output capacitors, and the other is the inductor current ripple charging and discharging the output capacitor. Ceramic capacitors with low ESR are strongly recommended for their small size and low output voltage ripple. Electrolytic and polymer capacitors may also be used. The output voltage ripple can be calculated by the following equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - D) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}})$$

where:

R_{ESR} is the equivalent series resistance of C_{OUT} in ohms (Ω).

For ceramic capacitors, the output voltage ripple can be calculated by the following equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - D)$$

Additionally, the temperature and DC bias voltage can both affect the capacitance. Ceramic capacitor can lose most of the capacitance at rated voltage. Therefore, use the X5R or X7R, and leave enough margin on the voltage rating to ensure the adequate effective capacitance and then to meet both load transient and output ripple performance. A minimum capacitance value of 2×22 μF is recommended. To compensate for the capacitance loss in ceramic capacitors under bias voltage, a capacitor with a voltage rating at least twice the maximum applied voltage should be selected.

SETTING VIN UNDER-VOLTAGE LOCKOUT (UVLO)

The AWK4573 has an internal, fixed UVLO threshold. The rising threshold is 3.4V, and the falling threshold is about 2.9V. At the same time, the device has a precision enable input that can be used to configure the UVLO threshold of the input voltage, which is showed by the Figure 56.

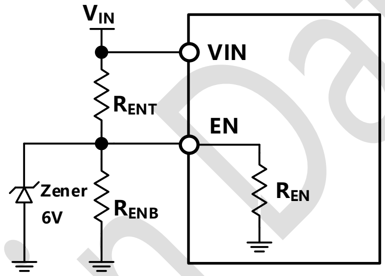


Figure 56. Configure the VIN UVLO

If enable (EN) control is on, then R_{EN} = 2.8MΩ. If EN control is off, then R_{EN} = 1.8MΩ. When EN is rising, the UVLO threshold can be calculated by the following equation:

$$V_{IN\_UV\_RISING} = (1 + \frac{R_{ENT}}{1.8M\Omega // R_{ENB}}) \times V_{EN\_RISING}$$

When EN is falling, the UVLO threshold can be calculated by the following equation:

$$V_{IN\_UV\_FALLING} = (1 + \frac{R_{ENT}}{2.8M\Omega // R_{ENB}}) \times V_{EN\_FALLING}$$

If the EN pin is connected to VIN through a resistor, for the EN pin's maximum ratings is 6V, add a 5.6V Zener diode between EN and GND. Meanwhile, R_{ENT} is required to be big enough to limit the current flowing into EN to below 100μA.

BOOTSTRAP (BST) RESISTOR AND CAPACITOR SELECTION

A resistor (R_{BST}) in series with C_{BST} can reduce SW's rising rate and voltage spikes. This improves EMI performance and reduces voltage stress at a high VIN. A higher resistance is better for SW spike reduction, but can compromise efficiency. To make a tradeoff between EMI and efficiency, it is recommended to keep R_{BST} below 20Ω. The recommended C_{BST} value is between 0.1μF and 1μF.

LAYOUT RECOMMENDATION

The quality of the PCB layout is essential for the performance of the AWK4573. Bad PCB layout can degrade the output regulation, the EMI and EMC performance. For the best performance the AWK4573, 4-layer layout is recommended to improve thermal performance, refer to Figure 57 and follow the guidelines.

1. Place the input capacitor, inductor, and output capacitor as close as possible to the IC, and use the short trace.
2. Place bypass capacitor for VCC close to the VCC pin.
3. Keep the switching loop as small as possible.
4. Keep VIN, VOUT, GND paths as short and wide as possible.
5. Place the feedback divider as close as possible to the FB pin to prevent noise pickup.
6. Place enough PCB area and use multiple vias to connect the power planes to the internal layer for proper heat sinking.

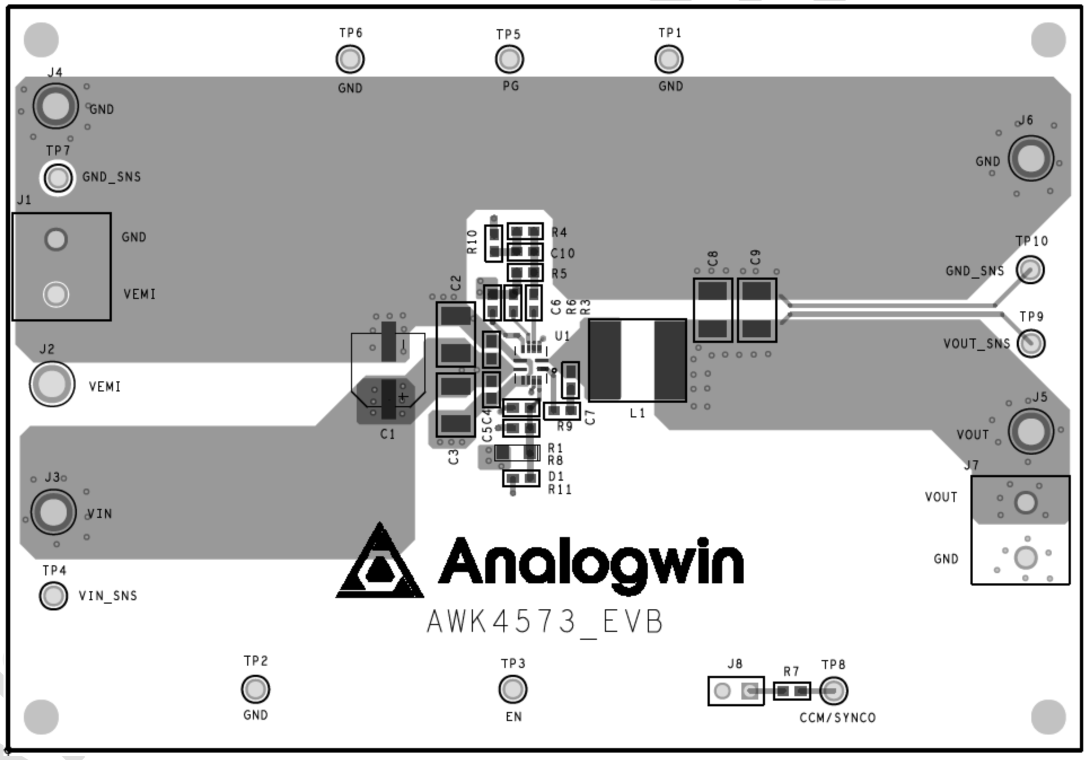


Figure 57. EVM TOP Layer Example

PACKAGE INFORMATION

PACKAGE TOP MARKING

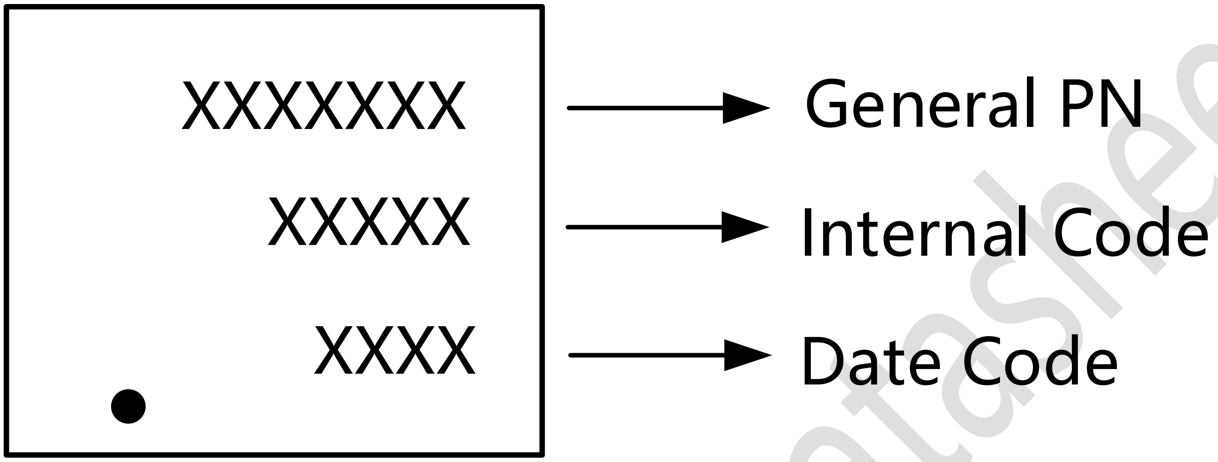


Figure 58. Package Top Marking

TAPE AND REEL BOX INFORMATION

DEVICE	PACKAGE TYPE	PACKAGE DRAWING	PINS	SPQ
AWK4573	QFN 2.5×3-12	TH	12	3000

TAPE AND REEL INFORMATION

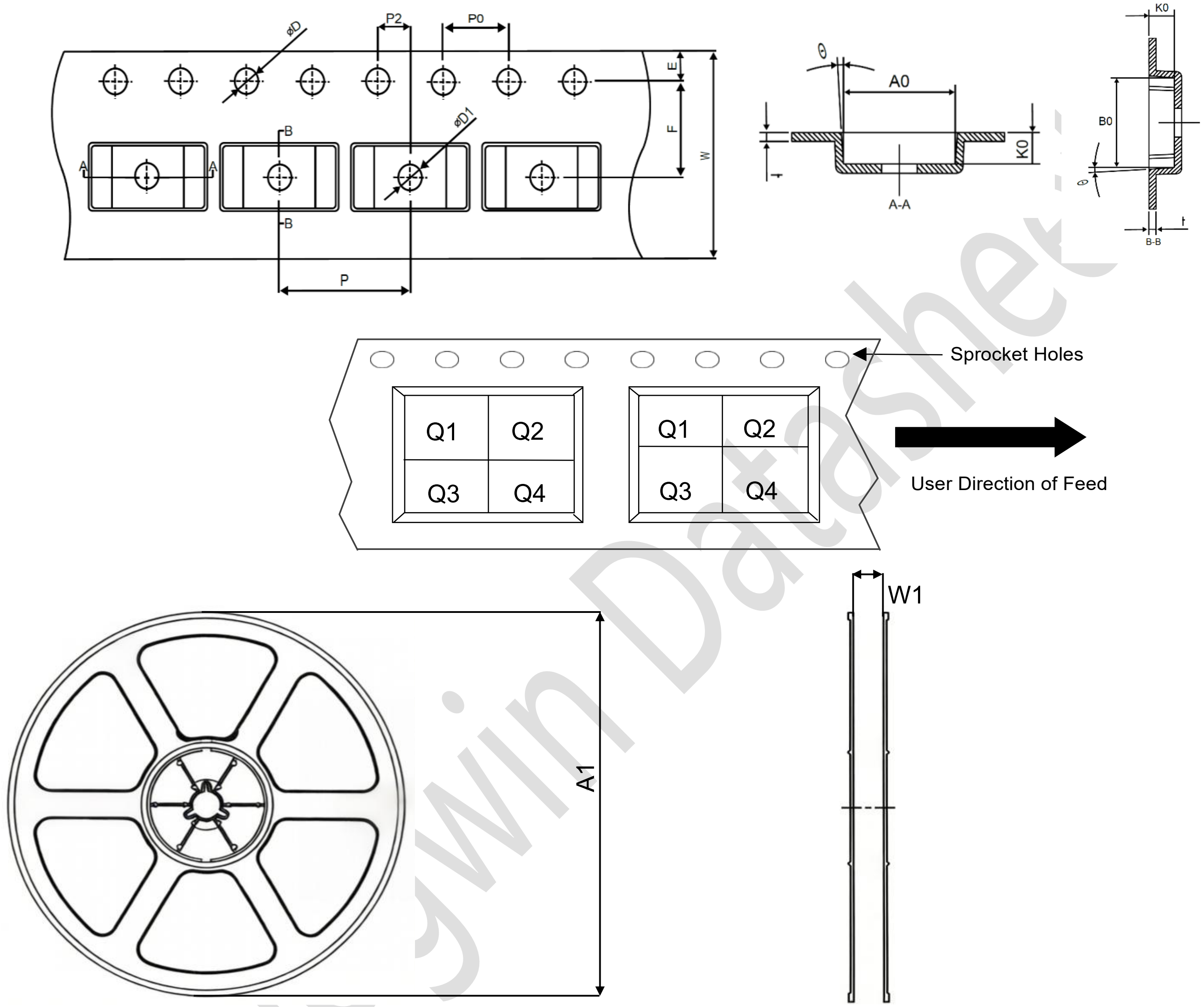


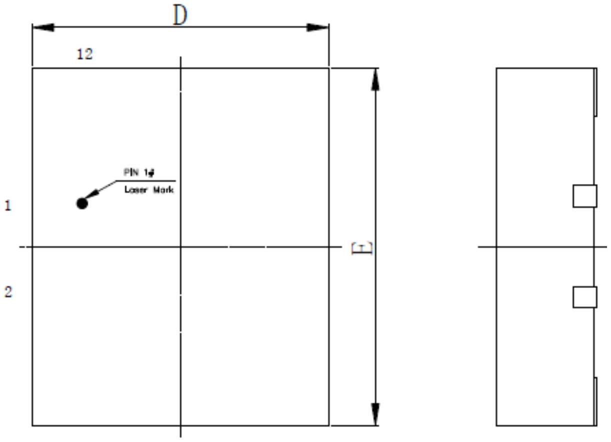
Figure 59. TAPE and Reel Information

DIMENSIONS AND PIN1 ORIENTATION

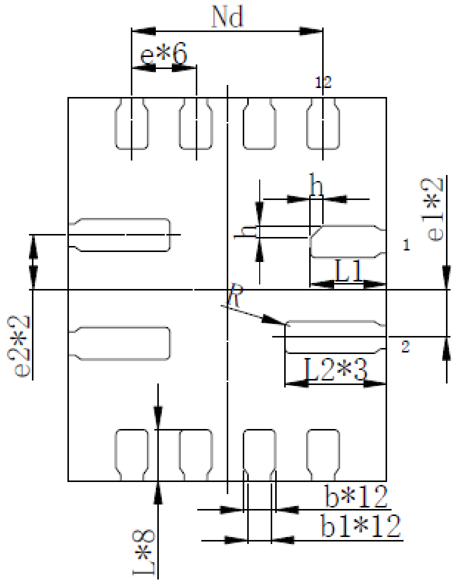
Device	Package Type	E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	W (mm)	W1 (mm)	P (mm)	A0 (mm)	A1 (mm)	B0 (mm)	K0 (mm)	t (mm)	Pin1 Quadrant	Quantity
AWK4573THR	QFN 2.5×3-12	1.75	5.50	2.00	1.55	1.10	4.00	12.0	12.8	8.00	2.80	180	3.3	1.20	0.25	Q1	3000

All dimensions are nominal

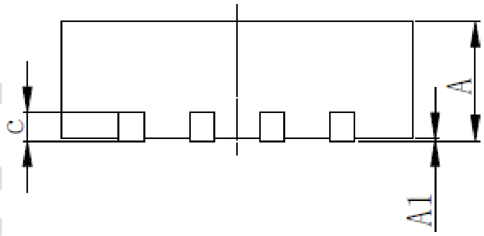
PACKAGE OUTLINES



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Figure 60. QFN 2.5×3-12 Package

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	2.40	2.50	2.60
e	0.50BSC		
e1	0.375BSC		
e2	0.425BSC		
E	2.90	3.00	3.10
Nd	1.50BSC		
L	0.35	0.40	0.45
L1	0.55	0.60	0.65
L2	0.75	0.80	0.85
h	0.05	0.10	0.15
R	0.04REF		

ORDERING INFORMATION

Device	Order Part No.	Load Current	Package	QTY
AWK4573	AWK4573THR	3A	QFN 2.5×3-12, Pb-Free	3000/Reel

REVISION HISTORY

Version	Date	Descriptions
Rev. 0.5	02/2026	Initial version