AWP1920

KEY FEATURES

- High-Voltage Low Power Piezo Driver
  - o Drives 10nF at 180Vpp and 200Hz sine wave with only **56 mW**
  - o Differential Output
  - o Small Solution Footprint, DFN 2x2-8L
- Low Quiescent Current: SHUTDOWN mode Current only 200 **nA**
- Wide Supply Voltage Range of **2.3V to 5.5V**
- Control Amplitude and Frequency through the PWM Duty Cycle
- Fast Start Up Time less than 700 μs

APPLICATIONS

- Micropump liquid cooling
- Portable injectable drug delivery system

GENERAL DESCRIPTION

The AWP1920 is a highly-integrated, piezo actuator driver. Capable of generating high-voltage waveforms up to 180 Vpk-pk from a low 2.3 to 5.5 V supply, it delivers precise actuation. Its ultra-low power consumption and compact size make it exceptionally well-suited for applications demanding strict power constraints.

The integrated differential driver architecture ensures exceptionally low distortion waveforms and near-silent actuator operation. Critically, the EN pin and FQ pin enable independent modulation of the output voltage amplitude and output frequency, respectively, via PWM signals.

The AWP1920 features ultra-fast startup capability with a typical time of under 700μs, introducing negligible latency in most systems.

Furthermore, the chip integrates comprehensive safety protection systems (including over-voltage, under-voltage, and over-temperature protections) to effectively prevent device damage under fault conditions.

TYPICAL APPLICATION

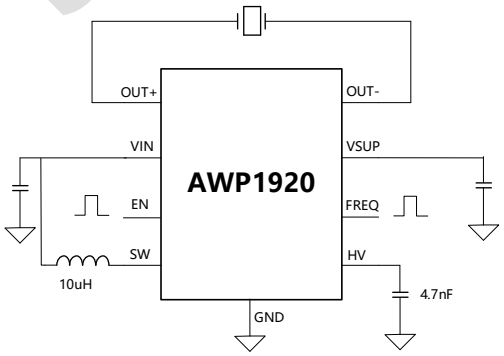


Figure 1. Typical Application Circuit

TABLE OF CONTENTS

PIN CONFIGURATION

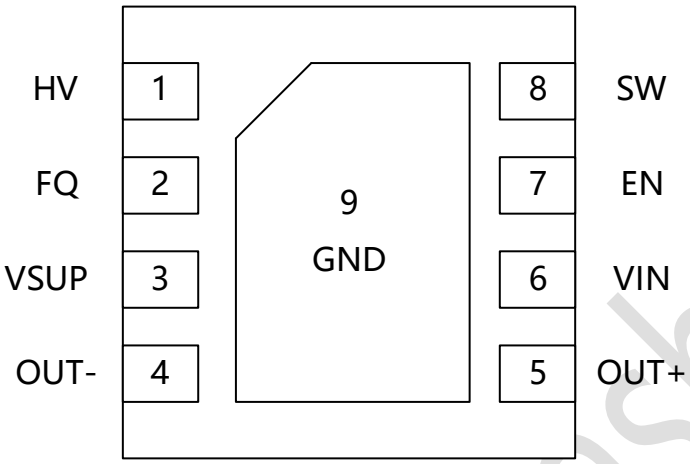


*Figure 2. DFN 2mm*2mm 8L package with exposed thermal pad (TOP VIEW; NOT TO SCALE)*

Table 1. DFN 8L Pin Function Descriptions

Pin No.	Pin Name	Type(1)	Description
1	HV	P	High-Voltage Output
2	FQ	I	Control frequency through the PWM duty cycle
3	VSUP	P	Supply Voltage
4	OUT-	O	Negative Differential Output
5	OUT+	O	Positive Differential Output
6	VIN	P	Main Power Supply
7	EN	I	Enable、Control amplitude through the PWM duty cycle
8	SW	P	Internal Power Converter Switch Pin
9	GND	P	Ground

(1) Legend: A = Analog Pin; P = Power Pin; D = Digital Pin; I = Input Pin; O = Output Pin.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Min	Max	Unit
Voltage at pins HV, OUT+, OUT-, SW	−0.3	110	V
Voltage at all other pins	−0.3	7	V
Junction temperature	−40	150	°C
Storage temperature	−65	150	°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 3.

Parameters	Min	Typ	Max	Unit
Operating Temperature	−40		125	°C
Continuous Supply Voltage (V_{IN})	2.3		5.5	V
Load Capacitance(1)			82	nF
Inductance		10		μH
Output frequency	50		250	Hz
Junction Temperature (T_J)	−40		125	°C

ELECTROSTATIC DISCHARGE (ESD)

Table 4. ESD Rating

Parameters	Description	Rating	Unit
HBM	Human Body Model ANSI/ESDA/JEDEC JS-001-2024 Classification, Class: 2	±2000	V
CDM	Charged Device Mode ANSI/ESDA/JEDEC JS-002-2025 Classification, Class: C2a	±500	V
Latch-Up	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±200	mA

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance

Item(1) (2)	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	TBD	°C/W
θ_{JC_Top}	Junction-to-case (top) thermal resistance	TBD	°C/W

(1) The package thermal impedance is calculated in accordance to JESD 51-7.

(2) Thermal Resistances were simulated on a 4-layer, JEDEC board.

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ELECTRICAL SPECIFICATIONS

V_{IN} = 3.6 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_J = 25°C of AWP1920AB for typical specifications, unless otherwise noted.

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Voltage at SUP pin	V_{sup}		2.10	2.30	2.50	V
Full-scale output voltage	$V_{OUT(FS)}$	AWP1920AB	168	180	192	V
VIN Shutdown current	I_{Q_VIN}	EN = 0V		200	1600	nA
Maximum Inductor Current	I_{L_MAX}			550		mA
Average VIN supply current during operation[1]	I_{VIN_AVG}	V_{IN} = 3.6 V f_{OUT} = 150 Hz V_{OUT} = 180 Vpk-pk C_{LOAD}= 82 nF		70		mA
		V_{IN} = 5.0 V f_{OUT} = 200 Hz V_{OUT} = 180 Vpk-pk C_{LOAD}= 10 nF		11.2		mA
Total Harmonic Distortion + Noise	THD+N	f_{OUT} = 150 Hz V_{OUT} = 180 Vpk-pk C_{LOAD} = 10 nF		0.25		%
Start-up Time[2]	T_start	EN is pulled up to the time when playback starts			700	μs
low-level input voltage	V_{IL}	FQ pin; EN pin			0.5	V
high-level input voltage	V_{IH}	FQ pin; EN pin	1.0			V
Recommended Duty Cycle of Amplitude (EN) [3] [4]	V_{OUT+} & V_{OUT-}	PWM=5%-10%		60		V_{PK_PK}
		PWM=20%-30%		90		V_{PK_PK}
		PWM=45%-55%		120		V_{PK_PK}
		PWM=70%-80%		150		V_{PK_PK}
		PWM=90%-100%		180		V_{PK_PK}
Recommended Duty Cycle of Frequency (FQ) [2] [3]	f_{OUT}	PWM=0%-10%		150		Hz
		PWM=20%-30%		100		Hz
		PWM=45%-55%		50		Hz
		PWM=70%-80%		250		Hz
		PWM=90%-100%		200		Hz

[1] This parameter is strongly correlated to the DCR of the inductor.
[2] This timing is related to the frequency setting
[3] The PWM frequency must exceed 200 kHz.
[4] The specific parameters for amplitude and frequency depend on the part number.

PRODUCT OVERVIEW

The AWP1920 is a highly integrated, single-chip piezo actuator driver. Capable of generating high-voltage waveforms up to 180 Vpk-pk from a low 2.3 to 5.5 V supply, it delivers precise actuation.
Its ultra-low power consumption and compact size make it exceptionally well-suited for applications demanding strict power constraints.

The integrated differential driver ensures exceptionally low distortion waveforms and near-silent actuator operation. Critically, the EN pin and FQ pin enable independent modulation of the output voltage amplitude and output frequency, respectively, through PWM signals.

The AWP1920 features ultra-fast startup capability with a typical time of under 700μs, introducing negligible latency in most systems.

Furthermore, the chip integrates comprehensive safety protection systems (including over-voltage, under-voltage, and over-temperature protections) to effectively prevent device damage under fault conditions.

FEATURE DESCRIPTION

EN

The EN pin supports two functional states. When held low, the device operates in Shutdown Mode, characterized by an ultra-low quiescent current with a typical value of 200nA, thereby ensuring minimal power consumption. When driven high, the device becomes active, and the internal circuitry utilizes the PWM control method applied through the EN pin to regulate the output amplitude. Depending on the duty cycle of the applied square-wave signal, the device operates in five distinct modes, as illustrated in the figure below.

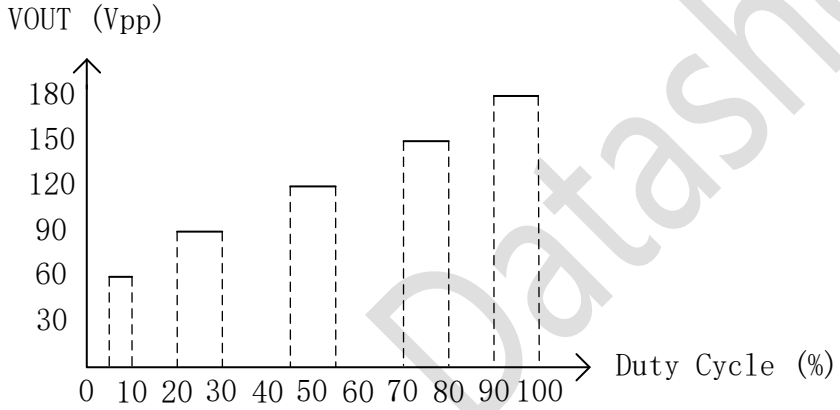


Figure 3. Output Voltage Vs PWM Duty Cycle

Do not leave EN pin floating.

FQ

The square-wave signal applied to the FQ pin regulates the output frequency through a PWM control scheme. Depending on the duty cycle of the applied square wave, the device operates in five distinct frequency modes, as illustrated in the figure below.

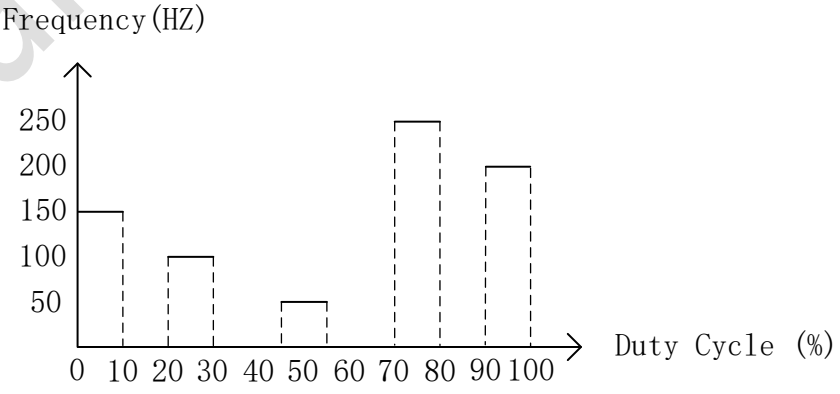


Figure 4. Output Frequency Vs PWM Duty Cycle

VSUP

The VSUP pin is the output of the internal LDO and is used to supply power to the internal analog circuitry. The VIN input is regulated by the LDO to generate a 2.3 V rail, which is provided as VSUP.

TYPICAL APPLICATION

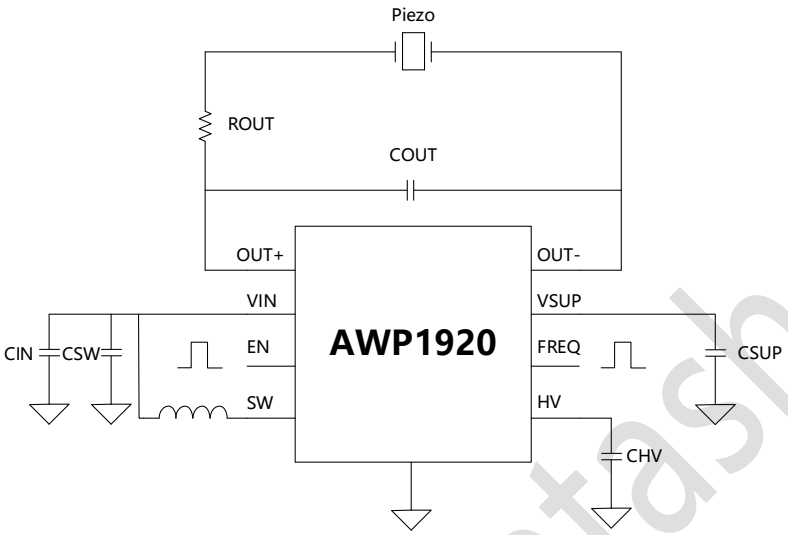


Figure 5. Typical Application Circuit

INDUCTOR SELECTION

Within the calculated range, a larger inductance value should be selected to reduce the switching frequency, thereby improving efficiency and minimizing EMI. However, it is important to note that higher inductance typically corresponds to higher DCR and larger dimensions, often requiring trade-offs. In this design, a 10 μH inductor is chosen.

INPUT CAPACITOR SELECTION

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (like X7R,C0G etc.) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. In this design, a 100nF capacitor is chosen.

VSUP CAPACITOR SELECTION

The VSUP pin supplies power to the internal analog circuitry. The VIN input is regulated through an internal LDO to generate a 2.3 V rail, provided as VSUP. To ensure stable operation of the internal analog circuits, a 100 nF decoupling capacitor should be placed between VSUP and GND.

CSW SELECTION

The SW pin and the VIN pin are tied to the same net. Because the SW node carries relatively large current, a capacitor should be placed at SW to stabilize the input voltage; use a low-ESR capacitor with a minimum capacitance of 10 μF. Note that energy accumulated on CSW can raise the input voltage; the resulting voltage increase must be controlled to ensure the total voltage does not exceed the absolute maximum rating of 5.5 V (VDD_max)。

CHV SELECTION

The capacitor on the HV pin should be increased appropriately as inductor current and load current increase. Typically, C_HV is selected as one-tenth of the load capacitance; if the calculated value is less than 4.7 nF, choose 4.7 nF as the minimum recommended value.

ROUT SELECTION

While the output waveform of our chip typically maintains a relatively low THD, higher-frequency components may still be present. To further mitigate noise through filtering, it is recommended to add a series resistor on either the OUT+ or OUT- line. The resistor value can be calculated with the below equation.

$$ROUT = \frac{1}{8 \times \pi \times C_{Piezo} \times f_{OUT}}$$

COUT SELECTION

In general, the chip design incorporates sufficient margin to drive most piezoelectric ceramics. However, for some ceramics with a high parasitic resistance, the output waveform may exhibit glitches. In such cases, it is recommended to stabilize the output loop by placing an MLCC capacitor in parallel at the output. An MLCC with a specification of 4.7 nF, 200 V is typically selected for this purpose.

PCB LAYOUT GUIDELINES

PCB layout is critical for stable operation of piezo driver AWP1920, especially for EMI design and Waveform THD. A four-layer layout is strongly recommended. However, to optimize cost, a two-layer PCB is sufficient to deliver the majority of the chip's performance. For best results, please refer to Fig.6 – Fig.7 and follow the guidelines below:

1. Place a low ESR ceramic capacitor as close to VIN, VSUP and HV pin and the ground as possible.
2. Place and route components inductor, input capacitor and HV capacitor close to each other to minimize area of the high di/dt current loop and reduce high voltage ringing & spikes.
3. Use a large ground plane to connect to PGND directly. And add vias near PGND.
4. Inductor should be placed close to the SW pin to minimize the SW area.
5. The CSW should be placed as close as possible to the input terminal of the inductor.
6. Keep SW node as small as possible.

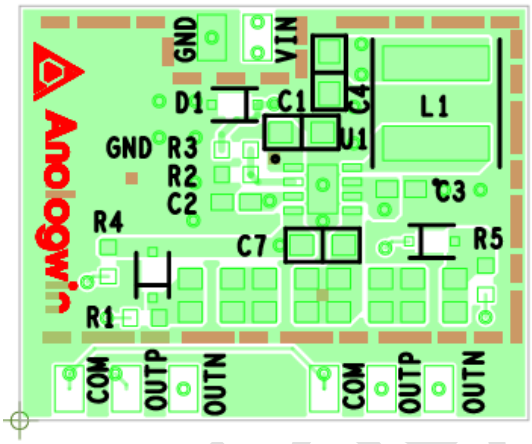


Figure 6. TOP Layout Example

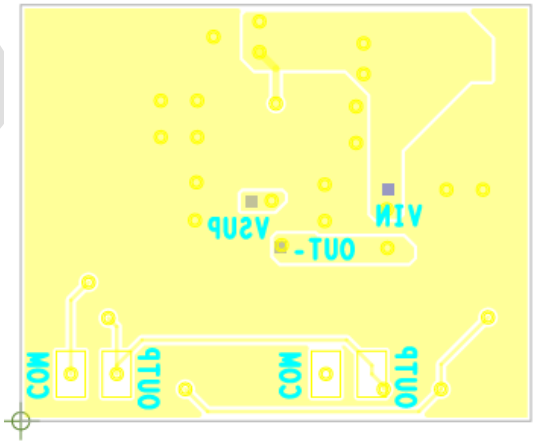


Figure 7. BOTTOM Layout Example

PACKAGE INFORMATION

PACKAGE TOP MARKING

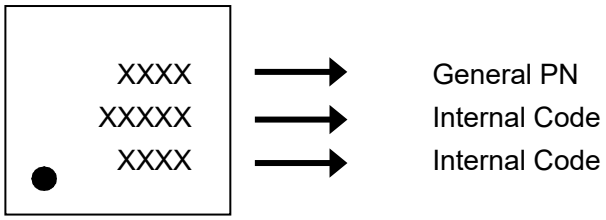


Figure 8. DFN2x2-8L Package Top Marking

TAPE AND REEL INFORMATION

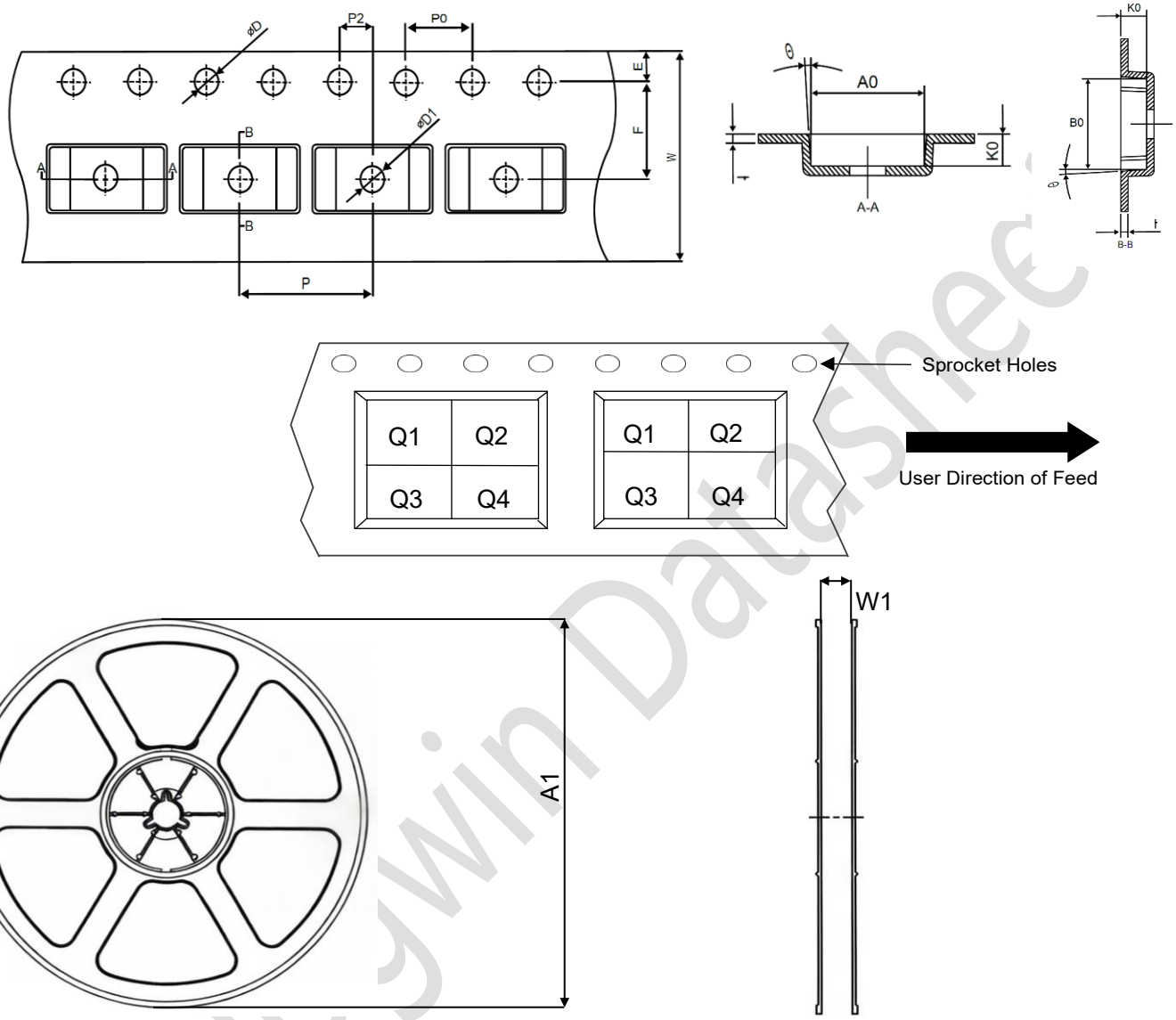


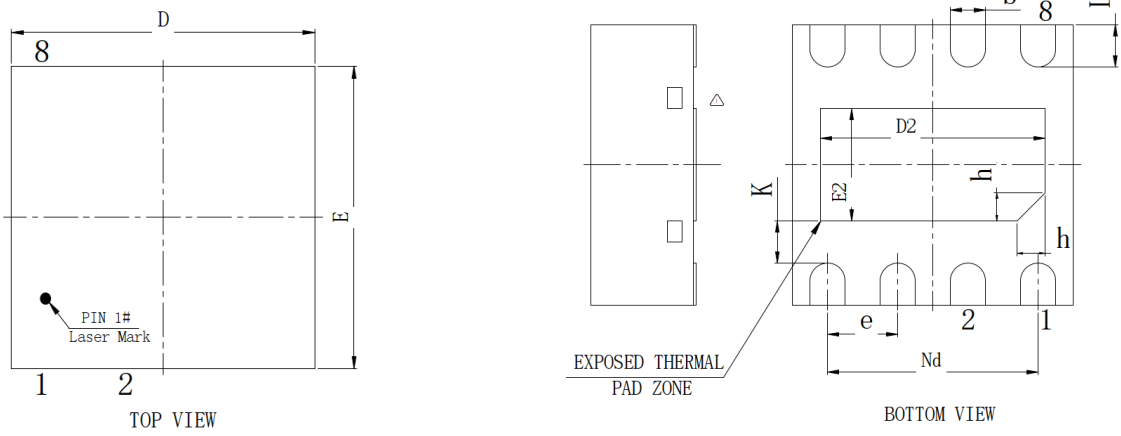
Figure 9. TAPE and Reel Information

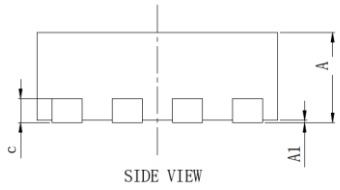
DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	W (mm)	W1 (mm)	P (mm)	A0 (mm)	A1 (mm)	B0 (mm)	K0 (mm)	t (mm)	Pin1 Quadrant	Quantity
AWP1920DBR	DFN2*2_8L	1.75	3.50	2.00	1.50	1.00	4.00	8.00	8.60	4.00	2.15	180	2.15	0.88	0.254	Q2	3000

All dimensions are nominal

PACKAGE OUTLINES





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.20	0.25	0.30
c	0.20REF		
D	1.95	2.00	2.05
D2	1.55	1.60	1.65
e	0.50BSC		
Nd	1.50BSC		
E	1.95	2.00	2.05
E2	0.75	0.80	0.85
L	0.25	0.30	0.35
K	0.25	0.30	0.35
h	0.20REF		

Figure 10.. DFN2x2-8L PKG

ORDERING INFORMATION

Device	Order Part No.	Inductor Current	Maximum Output Voltage	Package	QTY
AWP1920	AWP1920ABDBR	550mA	180Vpk-pk	DFN2x2-8L	3000/Reel
	AWP1920ACDBR	550mA	175Vpk-pk	DFN2x2-8L	3000/Reel

REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	01/2026	Initial Release.