



KEY FEATURES

- High-Voltage Low Power Piezo Driver
 - Drives 10nF at 180Vpp and 200Hz sine wave with only **64 mW**
 - Differential Output
 - Small Solution Footprint, DFN 2x2-10L
- Low Quiescent Current: SHUTDOWN mode Current only **350 nA**
- Wide Supply Voltage Range of **2.3V to 5.5V**
- Fast Start Up Time less than 700 μ s
- With I²C communication
- nINT pin supports event interrupt functionality

APPLICATIONS

- Micropump liquid cooling
- Portable injectable drug delivery system

GENERAL DESCRIPTION

The AWP1922 is a highly-integrated, piezo actuator driver. Capable of generating high-voltage waveforms up to 180 Vpk-pk from a low 2.3 to 5.5 V supply, it delivers precise actuation. Its ultra-low power consumption and compact size make it exceptionally well-suited for applications demanding strict power constraints.

The integrated differential driver architecture ensures exceptionally low distortion waveforms and near-silent actuator operation.

The AWP1922 features ultra-fast startup capability with a typical time of under 700 μ s, introducing negligible latency in most systems.

Furthermore, it supports I²C communication, enabling multi-level configuration of waveform frequency and amplitude. It integrates comprehensive safety protection systems. The settings and status of internal registers can be read via the I²C interface, and specific interrupt functions — such as UVLO, OVP, TSD — can be configured. If any fault is triggered, an interrupt alert is issued through the active-low nINT pin to effectively prevent device damage under fault conditions.

TYPICAL APPLICATION

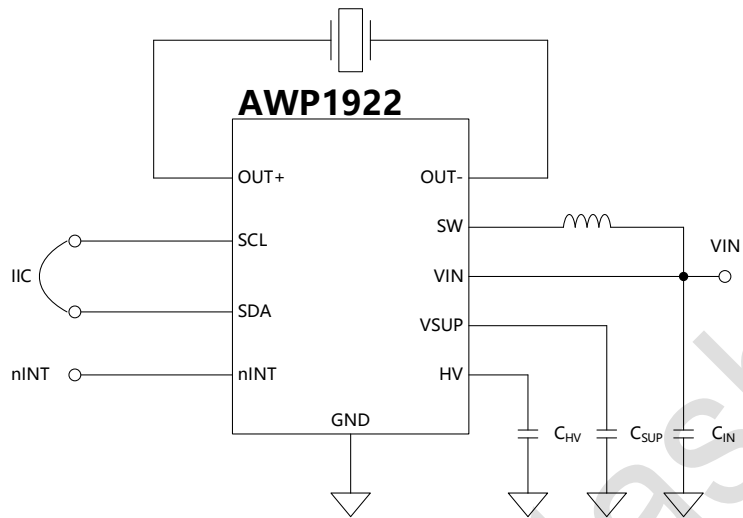
*Figure 1. Typical Application Circuit*

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PIN CONFIGURATION

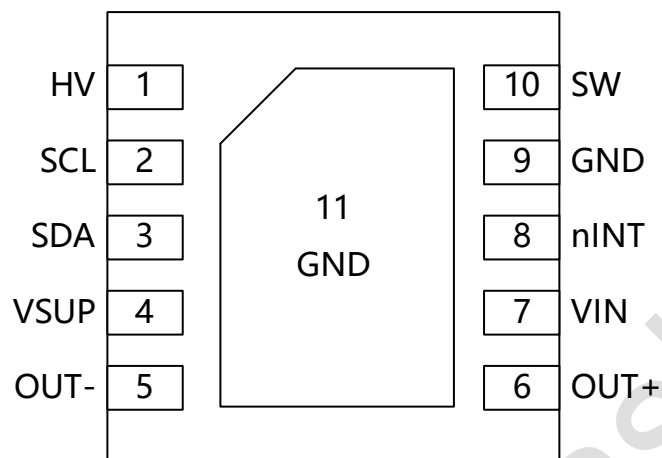


Figure 2. DFN 2mm*2mm 10L package with exposed thermal pad (TOP VIEW; NOT TO SCALE)

Table 1. DFN 10L Pin Function Descriptions

Pin No.	Pin Name	Type ⁽¹⁾	Description
1	HV	I/O	High-Voltage Output
2	SCL	I	I ² C clock
3	SDA	I/O	I ² C data
4	VSUP	P	Supply Voltage
5	OUT-	O	Negative Differential Output
6	OUT+	O	Positive Differential Output
7	VIN	P	Main Power Supply
8	nINT	O	Interrupt or Alarm Out Pin
9	GND	P	Ground
10	SW	I/O	Internal Power Converter Switch Pin
11	GND	P	Ground, Exposed Thermal Pad

(1) Legend: A = Analog Pin; P = Power Pin; D = Digital Pin; I = Input Pin; O = Output Pin.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Min	Max	Unit
Voltage at pins HV, OUT+, OUT-, SW	-0.3	110	V
Voltage at all other pins	-0.3	7	V
Junction temperature	-40	150	°C
Storage temperature	-65	150	°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 3.

Parameters	Min	Typ	Max	Unit
Operating Temperature	-40		125	°C
Continuous Supply Voltage (V_{IN})	2.3		5.5	V
Load Capacitance ⁽¹⁾			100	nF
Inductance		10		μH
Output frequency	25	200	375	Hz
Junction Temperature (T_J)	-40		125	°C

ELECTROSTATIC DISCHARGE (ESD)

Table 4. ESD Rating

Parameters	Description	Rating	Unit
HBM	Human Body Model ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
CDM	Charged Device Mode ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±500	V
Latch-Up	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±200	mA

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance

Item ^{(1) (2)}	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	TBD	°C/W
θ_{JC_Top}	Junction-to-case (top) thermal resistance	TBD	°C/W

(1) The package thermal impedance is calculated in accordance to JESD 51-7.

(2) Thermal Resistances were simulated on a 4-layer, JEDEC board.

ESD CAUTION



Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ELECTRICAL SPECIFICATIONS

$V_{IN} = 3.6\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ for minimum and maximum specifications, and $T_J = 25^\circ\text{C}$ for typical specifications, unless otherwise noted.

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Input Voltage	V_{IN}		2.30		5.50	V
Voltage at SUP pin	V_{SUP}		2.10	2.30	2.50	V
Full-scale output voltage ¹	$V_{OUT(FS)}$			180		V
Programmable Output playback frequency ¹	f_{OUT}	FERQ_SRATE [3:0] = 0x1111 FERQ_SRATE [3:0] = 0x0111 FERQ_SRATE [3:0] = 0x0000		375 200 25		Hz
V_{IN} Shutdown current	I_{Q_VIN}	EN = 0V		300	1600	nA
Maximum Inductor Current ¹	I_{L_MAX}			575		mA
Average V_{IN} supply current during operation ²	I_{VIN_AVG}	$V_{IN} = 3.6\text{ V}$ $f_{OUT} = 150\text{ Hz}$ $V_{OUT} = 180\text{ Vpk-pk}$ $C_{LOAD} = 82\text{ nF}$ $V_{IN} = 5.0\text{ V}$ $f_{OUT} = 200\text{ Hz}$ $V_{OUT} = 180\text{ Vpk-pk}$ $C_{LOAD} = 10\text{ nF}$		70 12.9		mA
Total Harmonic Distortion + Noise	THD+N	$f_{OUT} = 150\text{ Hz}$ $V_{OUT} = 180\text{ Vpk-pk}$ $C_{LOAD} = 10\text{ nF}$		0.25		%
Start-up Time ³	T_{start}	nINT is pulled up to the time when playback starts			700	μs
Digital low-level input voltage	V_{IL}				0.5	V
Digital high-level input voltage	V_{IH}		1.26			V
Digital low-level output voltage	V_{OL}	SDA, SCL, nINT pins			0.4	V
Digital high-level output voltage	V_{OH}		1.26			V

¹ This parameter is factory setting, please refer to the specific chip model in Ordering Information for details.

² This parameter is strongly correlated to the DCR of the inductor.

³ This timing is related to the frequency setting

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 3.6\text{ V}$, $T_J = 25^\circ\text{C}$, and the waveform being played is a 200Hz & 180V_{PK-PK} sine wave, unless otherwise noted.

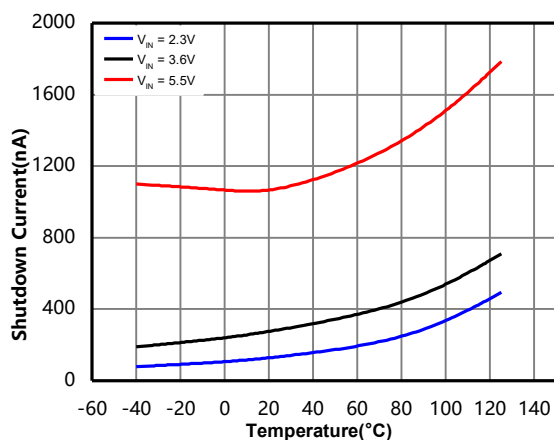


Figure 3. Shutdown Current Vs Temperature

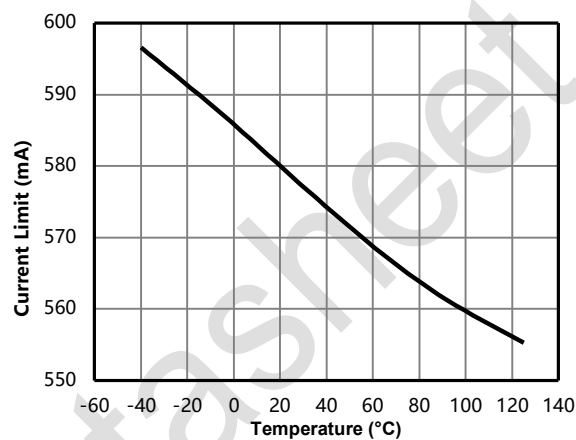


Figure 6. Current Limit Vs Temperature

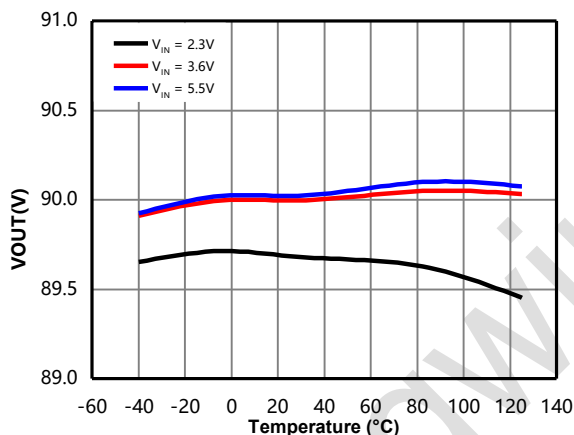


Figure 4. Maximum Output Voltage Vs Temperature

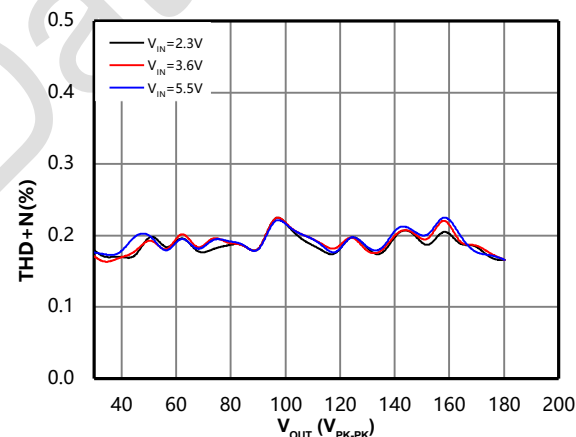


Figure 7. Total Harmonic Distortion + Noise vs Output Voltage

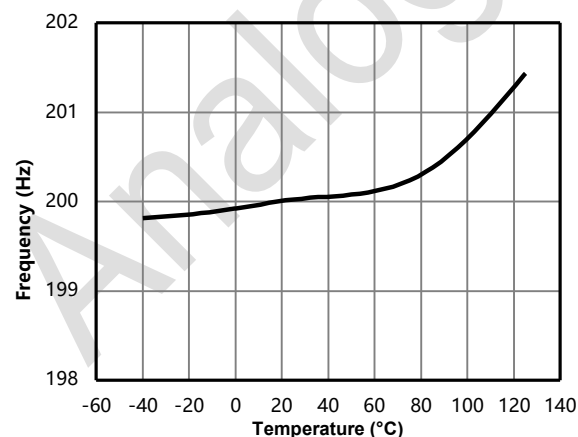


Figure 5. Output Frequency Vs Temperature

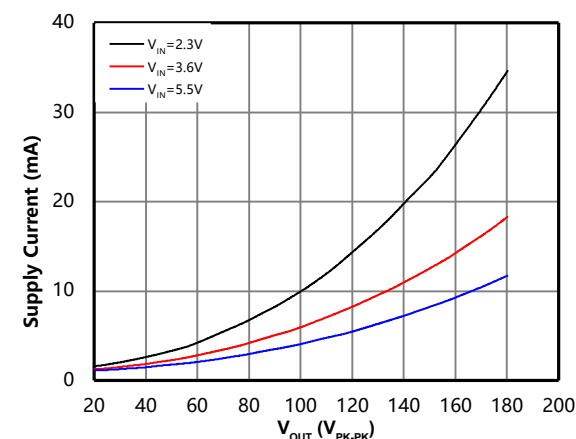


Figure 8. Supply Current vs Output Voltage

PRODUCT OVERVIEW

The AWP1922 is a highly integrated, single-chip piezo actuator driver. Capable of generating high-voltage waveforms up to 180 V_{PK-PK} from a low 2.3 to 5.5 V supply, it delivers precise actuation.

Its ultra-low power consumption and compact size make it exceptionally well-suited for applications demanding strict power constraints.

The integrated differential driver ensures exceptionally low distortion waveforms and near-silent actuator operation. Critically, the modulation of the output voltage amplitude and output frequency can modify the registers through the I²C

The AWP1922 features ultra-fast startup capability with a typical time of under 700μs, introducing negligible latency in most systems.

Furthermore, the chip integrates comprehensive safety protection systems (including over-voltage, under-voltage, and over-temperature protections) to effectively prevent device damage under fault conditions. The nINT pin is configured in an Open Drain structure and therefore requires a pull-up resistor to a high logic level. When an event is triggered, and if the corresponding interrupt has been enabled in the registers, this pin will notify the host by pulling low. Subsequently, the host can read register 0x01 to obtain detailed error information or the current operational status.

REGISTER MAP

Table 7.

ADDR	Bit	Default	Name	Type	Description
0x00	7	0x80	BIAS_EN	R/W	I ² C control enabled; when set to 0, the system enters shutdown mode.
	6		PLAY		If this bit is set to 1, playback begins
	5		RESERVE		RESERVE
	4				
	3				
	2		OTP_MASK	R/W	Status mask register 'Over Temperature Protection'
	1		OVP_MASK		Status mask register 'Over Voltage Protection'
	0		UVLO_MASK		Status mask register 'Under Voltage Lock Out'
0x01	7	0x00	RESERVE		RESERVE
	6		ON_PLAY	RO	Playback on-going
	5		RESERVE		RESERVE
	4				
	3				
	2		OTP	RO	Over Temperature Protection
	1		OVP		Over Voltage Protection
	0		UVLO		Under Voltage Lock Out
0x05	7	0x07 ¹	RESERVE		RESERVE
	6-4		I ² C_ADDR	RO	Determine the last three digits of the I ² C address
	3-0		FREQ_CONTROL[3:0]	R/W	Control the frequency of the output sine wave
0x06	7-5	0x00 ²	RESERVE		RESERVE
	4-0		VOUT_CONTROL[4:0]	R/W	Control the amplitude of the output sine wave

¹ The register value shown here is one possible value; the actual default value depends on the factory setting of the I²C_ADDR bit, which will be explained in detail in later sections.

² The register value shown here is one possible value; the actual default value depends on the factory setting of Plug-and-Play mode.

FEATURE DESCRIPTION

DIGITAL FRONT-END INTERFACE

The AWP1922 uses an I²C interface. This high-speed communication interface allows multiple ICs to share a common bus, so the chip is configured at the factory with different address bits for each model. This digital interface also provides access to internal registers, which can be used to start or stop waveform playback or to read the chip's status in real time.

I²C ADDR

The upper four address bits of the chip are fixed at '1011' by default. The remaining address bits are configured by bits 6-4 of the 0x05 register. For example, if the factory default setting for bit 6-4 is 010, the address is 1011010. This setting is factory-default and reverts to the default after power-off. When purchasing, please note the section on register addresses in the ordering information.

WAVEFORM SETTINGS

The AWP1922 can play only the sine waves stored in its ROM, but to accommodate different piezo actuators, we have reserved two internal registers for adjusting the waveform's frequency and amplitude. Once configured, simply send a playback command to the registers to play the waveform.

WAVEFORM AMPLITUDE

The output voltage of the AWP1922 can be adjusted via the 0x06 register, which uses bits 4 through 0. Each bit corresponds to a voltage of 2.82 V, with a minimum output of 2.82 V and a maximum output of 90 V.

WAVEFORM FREQUENCY

The output frequency of the AWP1922 can be adjusted via the 0x05 register, which occupies bits 3-0 of the register. Typically, each code word corresponds to a frequency difference of 25 Hz, meaning the minimum frequency is approximately 25 Hz and the maximum frequency is approximately 375 Hz. The factory default frequency is set to 200 Hz.

WAVEFORM PLAYBACK

Once the waveform has been configured, set bit 6 in the 0x00 register to 1 to start waveform playback. If you need to stop playback, clear this bit to 0.

PLUG-PLAY MODE

Since not all applications require communication with the host, some AWP1922 models come with Plug-Play functionality. In this case, the nINT pin is used as a playback enable pin. When the nINT pin is pulled high, the chip will immediately start playback using the factory default settings, at which point the nINT pin loses its original interrupt function.

INTERRUPT SYSTEM

The AWP1922 features an interrupt notification function. For non-Plug-Play chip models, the chip's nINT pin serves as the interrupt pin. By configuring register 0x00, the nINT pin can be pulled low to notify the host computer when a corresponding event occurs. Once the host computer receives the signal, it can determine which event has occurred by reading the contents of register 0x01. When using this pin, note that it is an open-drain structure and requires an additional pull-up resistor.

TRIGGER EVENTS ENABLED BY DEFAULT

The interruption includes event trigger: playback start; and error triggers: over temperature protection, over voltage protection, and undervoltage lockout. These three error events will execute protection actions regardless of whether masking is enabled. In the event of an error, if the mask is enabled, playback stops after the error is triggered and waits for I²C control to resume playback. If the mask is not enabled, playback stops during the error. Once the error ends, the device resumes playback from the beginning of sine waveform.

LOW QUIESCENT CURRENT

To address applications with stringent power consumption requirements, two low-power modes have been designed to accommodate varying needs.

IDLE MODE

By default, after power-on, the BIAS_EN bit in the chip's 0x00 register is set to high. At this point, operations such as I²C configuration and waveform generation can proceed normally, and waveforms can be started or stopped at any time as needed. When the device is not in operation, the current consumption is maintained at approximately 50 μ A at T_A=25°C.

SHUTDOWN MODE

When the BIAS_EN bit in register 0x00 is set to LOW, the I²C function is disabled, and the input current is limited to approximately 1 μ A at T_A=25°C. The previously configured register contents are retained as long as the VIN supply remains active. When I²C communication resumes, the BIAS_EN bit in register 0x00 is automatically set to HIGH, and the device returns to the IDLE state.

TYPICAL APPLICATION CIRCUIT

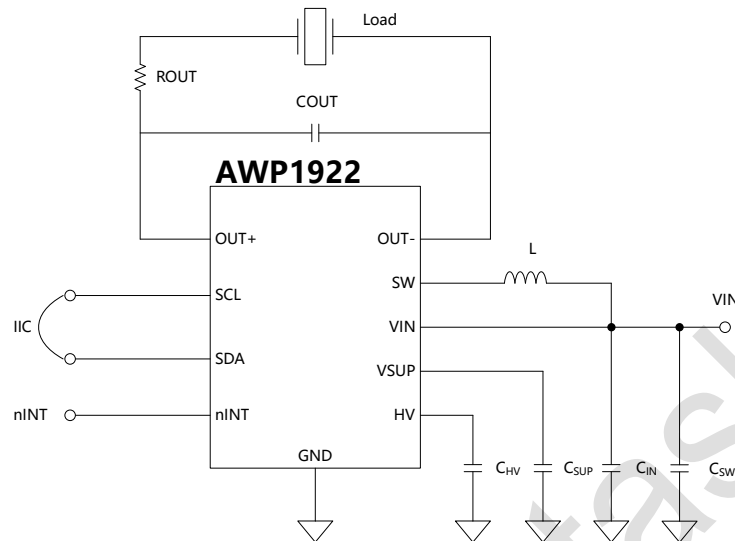


Figure 9. Typical Application Circuit

Table 8. Typical External Component Values

C_{IN}	C_{SW}	C_{SUP}	C_{HV}	C_{OUT}	R_{OUT}	L
1 μ F/10V + 100nF/10V	10 μ F/10V	100nF/10V	10nF/200V	4.7nF/200V	10k Ω	10 μ H

INDUCTOR SELECTION

Within the calculated range, a larger inductance value should be selected to reduce the switching frequency, thereby improving efficiency and minimizing EMI. However, it is important to note that higher inductance typically corresponds to higher DCR and larger dimensions, often requiring trade-offs. In this design, a 10 μ H inductor is chosen.

INPUT CAPACITOR SELECTION

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (like X7R,C0G etc.) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. In this design, a 100nF capacitor is chosen.

VSUP CAPACITOR SELECTION

The VSUP pin supplies power to the internal analog circuitry. The VIN input is regulated through an internal LDO to generate a 2.3 V rail, provided as VSUP. To ensure stable operation of the internal analog circuits, a 100 nF decoupling capacitor should be placed between VSUP and GND.

CSW SELECTION

The SW pin and the VIN pin are tied to the same net. Because the SW node carries relatively large current, a capacitor should be placed at SW to stabilize the input voltage; use a low-ESR capacitor with a minimum capacitance of 10 μ F. Note that energy accumulated on CSW can raise the input voltage; the resulting voltage increase must be controlled to ensure the total voltage does not exceed the absolute maximum rating of 5.5 V (VDD_max).

CHV SELECTION

The capacitor on the HV pin should be increased appropriately as inductor current and load current increase. Typically, C_{HV} is selected as one-tenth of the load capacitance; if the calculated value is less than 4.7 nF, choose 4.7 nF as the minimum recommended value. It should be noted that the recommended voltage rating for MLCCs is twice the maximum voltage of a single-sided output. For example, when playing a 180V_{PK-PK} waveform, it means that rated voltage close to 180V is required, so a nearby specification, 200V, should be chosen.

ROUT SELECTION

While the output waveform of our chip typically maintains a relatively low THD, higher-frequency components may still be present. To further mitigate noise through filtering, it is recommended to add a series resistor on either the OUT+ or OUT- line. The resistor value can be calculated with the below equation.

$$R_{OUT} = \frac{1}{8 \times \pi \times C_{piezo} \times f_{OUT}}$$

COUT SELECTION

In general, the chip design incorporates sufficient margin to drive most piezoelectric ceramics. However, for some ceramics with a high parasitic resistance, the output waveform may exhibit glitches. In such cases, it is recommended to stabilize the output loop by placing an MLCC capacitor in parallel at the output. A MLCC with a specification of 4.7 nF, 200 V is typically selected for this purpose.

LAYOUT RECOMMENDATION

PCB layout is critical for stable operation of piezo driver AWP1922, especially for EMI design and Waveform THD. A four-layer layout is strongly recommended. However, to optimize cost, a two-layer PCB is sufficient to deliver the majority of the chip's performance. For best results, please follow the guidelines below:

1. Place a low ESR ceramic capacitor as close to VIN, VSUP and HV pin and the ground as possible.
2. Place and route components inductor, input capacitor and HV capacitor close to each other to minimize area of the high di/dt current loop and reduce high voltage ringing & spikes.
3. Use a large ground plane to connect to PGND directly. And add vias near PGND.
4. Inductor should be placed close to the SW pin to minimize the SW area.
5. The CSW should be placed as close as possible to the input terminal of the inductor.
6. Keep SW node as small as possible.

PACKAGE INFORMATION

PACKAGE TOP MARKING

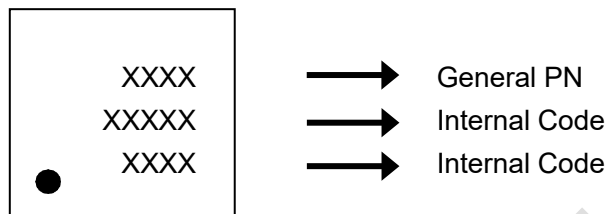


Figure 10. DFN2x2-10L Package Top Marking

TAPE AND REEL INFORMATION

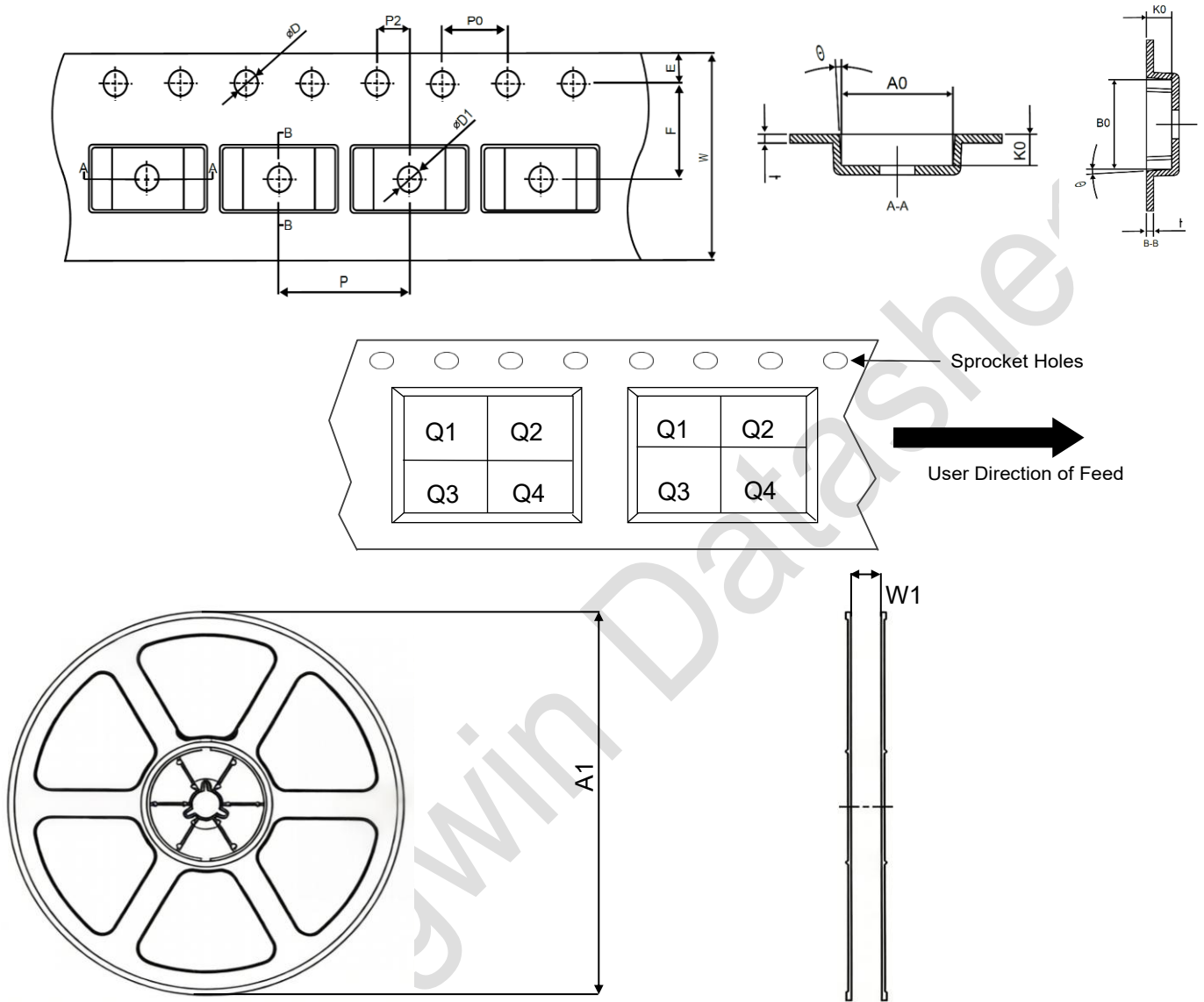


Figure 11. TAPE and Reel Information

DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	W (mm)	W1 (mm)	P (mm)	A0 (mm)	A1 (mm)	B0 (mm)	K0 (mm)	t (mm)	Pin1 Quadrant	Quantity
AWP1922DHR	DFN2*2_10L	1.75	3.50	2.00	1.50	1.00	4.00	8.00	8.60	4.00	2.15	180	2.15	0.88	0.254	Q2	3000

All dimensions are nominal

PACKAGE OUTLINES

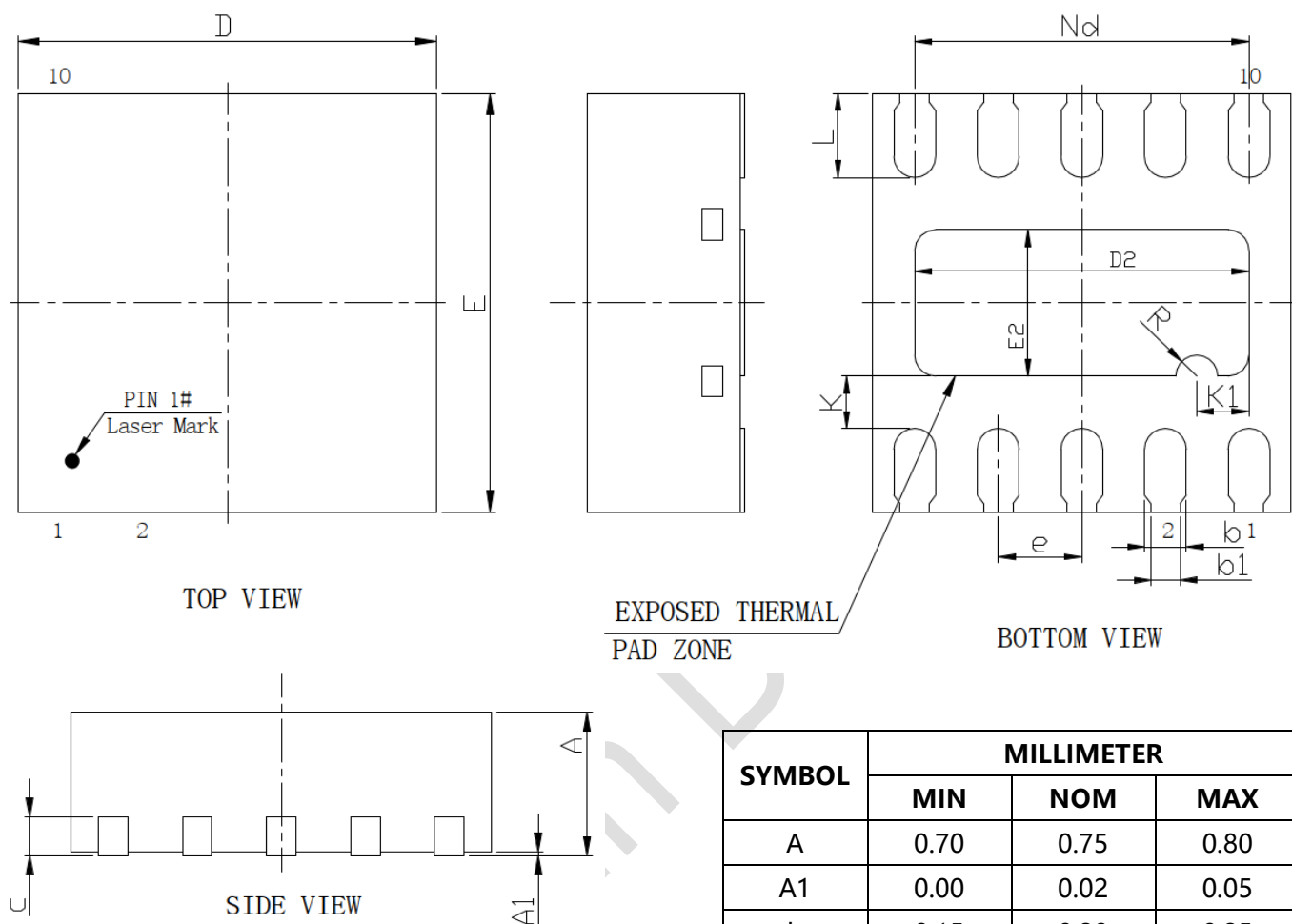


Figure 12. DFN2x2-10L PKG

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
b1	0.140REF		
c	0.203REF		
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
Nd	1.60BSC		
e	0.40BSC		
E	1.90	2.00	2.10
E2	0.60	0.70	0.80
L	0.30	0.40	0.45
K	0.250REF		
K1	0.250REF		
R	0.100REF		

ORDERING INFORMATION

Device	Order Part No.	Inductor Current	Maximum Output Voltage	Default Waveform Setting	nINT Function	Package	QTY
AWP1922	AWP1922AADHR	575mA	180Vpk-pk	120Vpk-pk 200Hz	Event Interruption	DFN2x2-10L	3000/Reel
	AWP1922ABDHR	575mA	180Vpk-pk	120Vpk-pk 200Hz	Plug-Play Enable	DFN2x2-10L	3000/Reel

REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	06/2026	Initial Release.